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(71) Applicants:
- **Halo LSI Design & Device Technology, Inc.**
  Wappinger Falls, NY 12590 (US)
- **New Halo Inc.**
  Tokyo 168-0072 (JP)

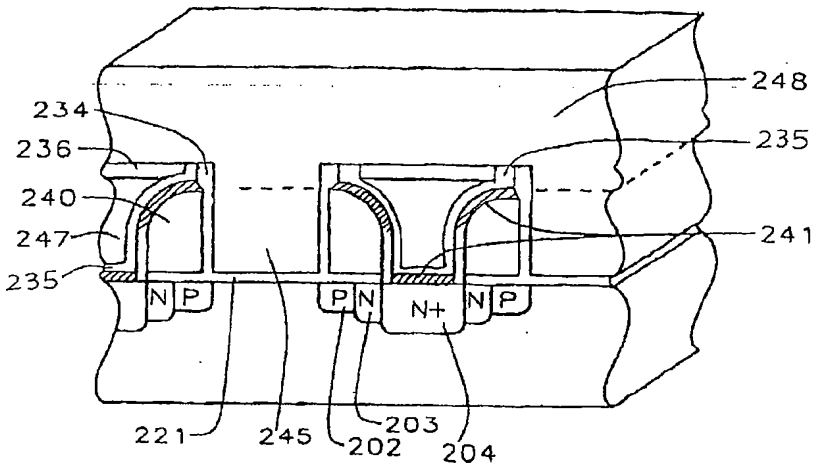
(72) Inventors:
- **OGURA, Seiki**
  Wappingers Falls, NY 12590 (US)
- **OGURA, Tomoko**
  Wappingers Falls, NY 12590 (US)
- **HAYASHI, Yutaka**
  Tsukuba-shi, Ibaraki 305-0045 (JP)

(74) Representative: **HOFFMANN EITLE**
Patent- und Rechtsanwälte
Arabellastrasse 4
81925 München (DE)

(54) DUAL BIT MULTI-LEVEL BALLISTIC MONOS MEMORY, AND MANUFACTURING METHOD, PROGRAMMING, AND OPERATION PROCESS FOR THE MEMORY

(57) In this invention, a fast low voltage ballistic program, ultra-short channel, ultra-high density, dual-bit multi-level flash memory is disclosed with a two or three polysilicon split gate side wall process and it operation. The structure and operation of this invention is enabled by a twin MONOS cell structure having an ultra-short control gate channel. The cell structure is realized by (i) placing side wall control gates (240) over a composite of Oxide-Nitride-Oxide (ONO) (230) on both sides of the word gate (245), and (ii) forming the control gates and bit impurity layer by self-alignment and sharing the control gates and bit impurity layers between neighboring memory cells for high density. Key elements used in this process are: 1) Disposable side wall process to fabricate the ultra short channel and the side wall control gate with or without a step structure, and 2) Self-aligned definition of the control gate over the storage nitride and the impurity layer.

Fig. 4F



EP 1 345 273 A1

Description

Technical Filed

[0001] The invention relates to methods of forming high-density Metal/polysilicon Oxide Nitride Oxide Silicon (MONOS) memory arrays and the resulting high density MONOS memory arrays.

Background Art

[0002] Floating gate and MONOS are two types of non-volatile memories. In conventional floating gate structures, electrons are stored onto a floating gate, by either F-N tunneling or source side injection. Conventional MONOS devices store electrons usually by direct tunneling in the Oxide-Nitride-Oxide (ONO) layer which is below the memory word gate. Electrons are trapped in the Nitride layer of the ONO composite. The MONOS transistor requires one less polysilicon layer than the floating gate device, which simplifies the process and could result in a denser array.

[0003] MONOS structures are conventionally planar devices in which an ONO composite layer is deposited beneath the word gate. The thickness of the bottom oxide of the ONO layer is required be less than 3.6nm, in order to utilize direct tunneling for program operations. However in 1998, a MONOS structure with a bottom oxide thickness of 5.0nm, and side wall polysilicon gates and source side injection program was first reported by Kuo-Tung Chang et al. in, "A New SONOS Memory Using Source Side Injection for Programming", IEEE Electron Letters, Vol. 19, No. 7, July 1998. In this structure, as shown in Fig. 1, a side wall spacer 20 is formed on one side of the word gate by a typical side wall process, and the ONO composite 22 is underneath the side wall gate, instead of under the word gate as for conventional MONOS memory cells. The channel under the SONOS side wall control gate is larger than 100nm, so the program mechanism is source side injection, which is faster and requires tower voltages than electron tunneling, despite the thicker bottom oxide. During source side injection, a channel potential is formed at the gap between the side wall gate and the select/word gate. Channel electrons 30 are accelerated in this gap region and become hot enough to inject into the ONO layer. Thus Kuo-Tung Chang's SONOS memory is able to achieve better program performance than previous direct tunneling MONOS cells.

[0004] While the SONOS memory cell is unique among MONOS memories for its split gate structure and source side injection program, its structure and principles of program are similar to those for a conventional split gate floating gate device. Both cell types have a word gate and side wall spacer gate in series. The most significant differences lie in the manner of side wall gates utilization and electron storage regions. In the split gate floating gate cell, the side wall spacer is a floating gate onto which electrons are stored. The floating gate voltage is determined by capacitance coupling between the word gate, diffusion, and floating gate. For the SONOS cell, electrons are stored in the nitride region beneath the side wall spacer, which is called the control gate. The nitride region voltage is directly controlled by the voltage of the above side wall gate.

[0005] A floating gate memory cell having faster program and higher density was introduced in co-pending U.S. Patent Application Serial Number 09/313,302 to the same inventors, filed on May 17, 1999. Fig. 3A is an array schematic and Fig. 3B is a layout cross-section of this fast program, dual-bit, and high density memory cell. In this memory structure, high density is achieved by pairing two side wall floating gates to one word gate (for example, floating gates 312 and 313 and word gate 341), and sharing interchangeable source-drain diffusions (321 and 322) between cells. Thus a single memory cell has two sites of electron storage. Additional polysilicon lines, "control gates" run in parallel to the diffusions and orthogonal to the word gates. The control gates (331 and 332) couple to the floating gates and provide another dimension of control in order to individually select a floating gate from its pair. This memory is further characterized by fast programming due to ballistic injection. Using the same device structure, if the side wall gate channel is reduced to less than 40nm with proper impurity profiles, the injection mechanism changes from source side injection to a new and much more efficient injection mechanism called ballistic injection. The ballistic injection mechanism has been proven by S. Ogura in "Step Split Gate Cell with Ballistic Direction Injection for EEPROM/Flash", IEDM 1998, pp.987. In Fig. 2A, results between ballistic injection (line 25) and conventional source side injection (line 27) are compared for a floating gate memory cell. Although the structures are very similar, when the control gate is 100nm, the injection mechanism is source side injection. However, as illustrated in Fig. 2B, when the channel is reduced to 40nm to satisfy the short channel length requirement for ballistic injection (line 35), program speed increases by three orders of magnitude under the same bias conditions, or at half of the floating gate voltage requirement for source side injection (line 37).

[0006] In contrast, the side wall channel length of Kuo Tung Chang' s SONOS memory structure is 200nm, so the program mechanism is source side injection. Thus there is a significant dependence between the short channel length and the injection mechanism.

Disclosure of Invention

[0007] In this invention, a fast low voltage ballistic program, ultra-short channel, ultra-high density, dual-bit multi-level flash memory is achieved with a two or three polysilicon split gate side wall process. The structure and operation of this invention is enabled by a twin MONOS cell structure having an ultra-short control gate channel of less than 40nm, with ballistic injection (S. Ogura) which provides high electron injection efficiency and very fast program at low program voltages of 3-5V. The cell structure is realized by (i) placing side wall control gates over a composite of Oxide-Nitride-Oxide (ONO) on both sides of the word gate, and (ii) forming the control gates and bit diffusion by self-alignment and sharing the control gates and bit diffusions between memory cells for high density. Key elements used in this process are;

(i) Disposable side wall process to fabricate the ultra short channel and the side wall control gate with or without a step structure channel.
(ii) Self-aligned definition of the control gate over the storage nitride and the bit line diffusion, which also runs in the same direction as the control gate.

[0008] The features of fast program, low voltage, ultra-high density, dual-bit, multi-level MONOS NVRAM of the present invention include;

1. Electron memory storage in nitride regions within an ONO layer underlying the control gates.
2. High density dual-bit cell in which there are two nitride memory storage elements per cell
3. High density dual-bit cell can store multi-levels in each of the nitride regions
4. Low current program controlled by the word gate and control gate
5. Fast, low voltage program by ballistic injection utilizing the controllable ultra-short channel MONOS
6. Side wall control poly gates to program and read multi-levels white masking out memory storage state effects of the unselected adjacent nitride regions and memory cells.

[0009] The ballistic MONOS memory cell is arranged in the following array; each memory cell contains two nitride regions for one word gate, and 1/2 a source diffusion and 1/2 a bit diffusion. Control gates can be defined separately or shared together over the same diffusion. Diffusions are shared between cells and run in parallel to the side wall control gates, and perpendicular to the word line.

[0010] A summary of the operating conditions for multi-level storage is given in Fig. 3B. During read, the following conditions need to be met; the voltage of the unselected control gate within a selected memory cell must be greater than the threshold voltage of the control + source voltage. The word select gate in the control gate pair is raised to the threshold voltage of the word gate + an override delta of around 0.5V + source voltage (Vt-wl + V overdrive + Vs). unselected MONOS cells wilt be disabled by reducing the associated control gates to 0V. Program conditions are; Word line voltage is greater than threshold + an overdrive voltage delta for low current program. Both control gates in the selected pair are greater than Vt-high (the highest threshold voltage within the range of multi-level thresholds) + override delta. Adjacent memory cells sharing the same word line voltage are disabled by adjusting the control gates only.

Brief Description of Drawings

[0011]

Fig. 1 is a device structure of prior art SONOS (Silicon Oxide Nitride Oxide Silicon).
Fig. 2A graphically represents empirical results for a split gate floating gate transistor, demonstrating that for a channel length of 100nm, source side injection requires high voltage operation.
Fig. 2B graphically represents empirical results for a split gate floating gate transistor showing that for a channel length of 40nm, ballistic injection operates at much lower voltages and/or much faster program speed.
Fig. 3A is an array circuit of the prior art double side wall dual-bit split floating gate cell with ultra short ballistic channel.
Fig. 3B is a layout cross-section of the prior art double side wall dual-bit split floating gate cell with ultra short ballistic channel.
Figs. 4A through 4F are cross sectional representations of a first preferred embodiment of the process of the present invention.
Fig. 4G is a bird eye's view of the completed memory cell of the present invention.
Figs. 5B, 5C, and 5F are cross sectional representations of a second preferred embodiment of the process of the present invention.

Figs. 6A through 6D and 6F are cross sectional representations of a third preferred embodiment of the process of the present invention.

Fig. 7A is an array circuit of the present invention.

Fig. 7B is a cross-sectional representation of the present invention.

Figs. 7C and 8A give the required voltage conditions during read for the present invention.

Fig. 8B is graphical representation of voltage sensing curves for the present invention during read.

Fig. 8C is graphical representation of voltage/current sensing curves for the present invention during read.

Best Mode for Embodying the Invention

[0012] Presented in this invention is a fabrication method for a ballistic twin MONOS memory cell with two nitride memory elements and two shared control gates . The method can be applied to a device with a flat channel and/or a device having a step channel under the nitride layer in the MONOS cell.

[0013] The procedures for formation of shallow trench isolation, p-well, and n-well are the same as for conventional CMOS processing and will not be shown. The polysilicon word gate is also defined by conventional CMOS processing as shown in Fig. 4A. In order to define the word gate, the memory gate silicon oxide 221 is formed to a thickness of between about 5 and 10 nanometers. Then the polysilicon 245 with a thickness of between about 150 and 250 nm for the gate material is deposited by chemical vapor deposition (CVD). A nitride layer 232 is deposited by CVD to a thickness of between about 50 and 100nm to be used later as an etch stop layer for chemical mechanical polishing (CMP). Normal CMOS processing defines the memory word gates; i.e., photoresist and masking processes with exposure, development, and vertical etching of the nitride 232 and polysilicon 245 by reactive ion etching (RIE) are performed. Extra boron 202 is ion implanted at low energy (less than about 10KeV energy) with an ion dosage of between 3E12 to 3E13 ions per cm^2, in order to adjust VT under the floating gate. After removing the photoresist which was used to define the word gate, the word gate is obtained as shown in Fig 4A.

[0014] A thin silicon oxide layer 234 of between about 5 and 10 nm can be thermally grown on the side wall polysilicon, or SiO_2 and/or SiN film can be deposited by uniform CVD, as shown in Fig 4B. Then the disposable sidewall process, which defines a controllably short channel and provides fast programming by high electron injection efficiency, is performed. A thin Polysilicon layer typically having a thickness of between about 30 to 50 nm is deposited. Then a vertical or anisotropic polysilicon etch is performed, which forms the disposable sidewall spacer 242 on both sides of the word gate 245, as shown in Fig.4B. Implantation with an N dopant 203 such as arsenic is performed with an ion dosage of between 3E13 and 4E13/cm^2 at 10 to 15KeV. Thus, the thickness of the polysilicon layer determines the effective channel length under the control gate.

[0015] Referring now to Fig. 4C, the disposable side wall spacer 242 is gently removed by a dry chemical anisotropic etch. A typical etch ambient for this step is $HBr/Cl_2/O_2$. The bottom silicon oxide 221 is then gently etched out by buffered (with for example water of ammonium hydroxide) hydrofluoric acid (BHF). Vapor HF, or a reactive ion etch such as CF_2/O_2. A composite layer of oxide-nitride-oxide 230 is formed. Layer 230 is shown without the three layers for simplicity. The bottom oxide is thermally grown and the thickness is between 3.6 and 5 nm, which is slightly thicker than the limit of direct tunneling (3.6nm), the silicon nitride layer deposited by chemical vapor deposition is about 2 to 5 nm, and the top oxide is deposited by CVD deposition and is between about4 and 8 nm. Thermal oxidation may be added to improve the top oxide quality. Also short nitridation in an N_2O environment can be added to improve the bottom oxide reliability prior to the deposition of the nitride layer.

[0016] Now, an insitu phosphorus-doped thin polysilicon layer between about 30 and 50 nm and tungsten silicide between 60 and 100 nm is deposited by CVD. The composite layer of polysilicon and tungsten silicide becomes the control sidewall spacer gate. A vertical, anisotropic reactive etch is performed to form the sidewall control gate 240, as shown in Fig. 4C. The composite oxide-nitride-oxide layer is also etched through, leaving this ONO layer 230 only underlying the sidewall control gates.

[0017] A thin CVD of silicon oxide or nitride 233 with a thickness Of about 10nm is deposited. Phosphorus and/or Arsenic for n+ junction 204 is implanted subsequently, at a dosage of between 3E14 to 5E15 ions per cm^2, as shown in Fig.4C. The total thickness is between 90 to 150 nm, which is equal to the summation of effective control gate channel length and lateral out diffusion of the n+ junction.

[0018] As an option, the sidewall spacer gate 240 can be simply an insitu phosphorus or As doped polysilicon layer instead of the composite layer of polysilicon and tungsten silicide. After the formation of the n+ junction and the deposition of a thin CVD of silicon oxide or nitride 233 with a thickness of about 10 nm, the vertical reactive ion etch is performed to form sidewall oxide spacer 233 on the gate 240 when the control gate requires low resistivity and silicidation, as shown in Fig. 4D. In typical silicidation, about 10nm Co or Ti is deposited by plasma sputtering and a Rapid Thermal Anneal at about 650 °C is performed. The formation of silicide layer 241 on the top part of gate 240 and diffusion 204 are shown in Fig 4D. Although silicidation 241 is shown in Fig. 4D, it is not required. It is an option to reduce the RC time constant of the control gate lines or diffusion lines in order to improve performance in all modes

of operation, read, program, and erase.

[0019] An oxide and/or nitride layer 235 for contamination barrier is deposited by CVD. Then a layer of CVD silicon oxide or BSG 247 is deposited to fill the gap. The gap fill material is polished by CMP up to the nitride layer 232.

[0020] As an option, the gap fill material 247 can be a conductive material like polysilicon or W, which can be used for reducing the RC time constant of the sidewall gate or bit diffusion depending on the need. When the conductive layer is polished by CMP up to the nitride layer 232, the conductive layer is several hundred nanometers (50nm) recessed by vertical reactive ion etch. Then a CVD SiO_2 layer (about 50nm) is deposited and CMP is performed as illustrated by 236 as shown in Fig 4E.

[0021] The nitride layer 232 in Fig. 4E is selectively etched by H_3PO_4 or etched by a chemical dry etch. The polysilicon layer thickness of between 150 and 200 nm is deposited by CVD. This polysilicon layer 248 and the underlying polysilicon word gate 245 are defined by normal photoresist and RIE processes. The structure at this point is as shown in Fig. 4F.

[0022] The polysilicon layer 248 acts as a word line wire by connecting adjacent word line gates. The final memory cell is completed at this point. This word polysilicon layer can be silicided with Ti or Co to reduce the sheet resistance. A typical bird's-eye view of the memory cell is shown in Fig 4G. The shallow trench isolation region is shown by area 209 in Fig. 4G.

[0023] The preceding processes describe fabrication of planar channel twin MONOS memory with very short channel (30 to 50 nm). By modifying and adding a few process steps, a step split structure with more efficient ballistic injection can be fabricated using the same process integration scheme as the planar structure. This second embodiment of the present invention will be described with reference to Figs. 5B, 5C, and 5F.

[0024] After forming disposable sidewall spacer 242 by etching vertically the doped polysilicon, the silicon oxide layer 221 is vertically etched which corresponds to Fig 4B. In order to form a step split memory cell, the deviation starts at this point by continuing to etch into the silicon substrate by approximately 20 to 50 nm. Then the bottom of the step is lightly implanted with Arsenic to form N-region 203 using the poly sidewall as a mask as shown in Fig 5B, where the dosage is about 3E13 to4E13 /cm^2 at 10 to 15 KeV. Next, the N+ doped polysilicon disposable spacer is selectively removed by a wet etch (HNO_3/HF/Acitic acid, or H_3PO_4 or NH_4OH) or a dry plasma etch to the lightly doped bulk N-region. The bulk etching during this disposable spacer etch can be included as part of step etching. After gently etching off the left over gate oxide 221 under the disposable polysilicon spacer, the silicon surface is cleaned. The total step into silicon should be about 20 to 50 nm. If the step corner is sharp, corner rounding by rapid thermal anneal (RTA) at between about 1000 to 1100 °C for about 60 seconds can be added as an option or a hydrogen anneal at 900°C and at a pressure of 200 to 300 mtorr can be performed. After these modifications and additions, the fabrication sequence returns to the procedures described previously.

[0025] Referring to Fig. 5C, a composite layer of oxide-nitride-oxide is formed. Layer 230 is shown without the three layers for simplicity. The bottom oxide is thermally grown and the thickness is between 3.6 and 5 nm, which is slightly thicker than the limit of direct tunneling (3.6nm), the silicon nitride layer deposited by chemical vapor deposition (CVD) is about 2 to 5 nm, and the top oxide is deposited by CVD deposition and is between about 4 and 8 nm. Thermal oxidation may be added to improve the top oxide quality. Also, short nitridation in an N_2O environment can be added to improve the bottom oxide reliability prior to the deposition of the nitride layer.

[0026] Then an insitu phosphorous-doped polysilicon layer, which becomes the control gate, is deposited having a thickness of between 90 to 180 nm, and a vertical or anisotropic polysilicon etch is performed to form the sidewall gate 240, a shown in Fig 5C. By following the process steps given for the planar split device, the step-split device can be fabricated as shown in Fig 5F. This sidewall polysilicon gate can be silicided or replaced by refractory silicide as utilized in the first embodiment of the flat channel MONOS twin cell.

[0027] In the above process steps for both the planar and step devices, the disposable side wall spacer 242 can be plasma nitride or oxynitride or Boron Phosphorus Silicate Glass (BPSG) instead of polysilicon, since the etching rate of that material to the thermal silicon oxide can be very high (for example at least 10-100 times) in H_3PO_4 acid or diluted HF.

[0028] A third embodiment of the present invention will be described with reference to Figs. 6A-6D and 6F. The third embodiment of the present invention will be a simplified process of the first embodiment of the planar twin MONOS memory cell with a slight program speed penalty because controllability will be lost due to the usage of a single large spacer instead of two side wall spacers. Deviation from the normal CMOS process starts prior to deposition of word gate polysilicon 245. A composite layer of oxide-nitride-oxide (ONO), 230 in Fig 6A, is formed. Layer 230 is again shown without the three layers for simplicity. The bottom silicon oxide layer is preferred to be grown thermally with a thickness of between about 3.6 to 5 nm, the silicon nitride layer deposited by CVD deposition is about 2 to 5 nm and the top oxide layer is deposited by CVD deposition and about 5 to 8 nm thick. The top oxide CVD layer is slightly thicker compared to the first and second process embodiments, for subsequent polysilicon and disposable sidewall spacer etch stop. Then the polysilicon 245 for gate material is deposited by CVD and followed by CVD silicon nitride 232 deposition thickness of between about 50 to 100 nm.

[0029] Then a photoresist layer is formed and a masking process with exposure and development to define memory gates 245 are performed. The polysilicon layer is now etched vertically by reactive ion etching (RIE), using the under layer top silicon oxide in the composite layer 230 as a etch stop. Then extra boron 202 is ion implanted at low energy (less than 10keV power and ion dosage of between about 5E12 to 2E13 ions per cm^2, also shallow As is implanted at the same time at about 5E12 to 1.5EI3 at the same KeV range as is the boron, as shown in Fig. 6A. Even though the channel threshold is very low due to As compensation, there is plenty of impurity to create a channel potential drop in the short channel region.

[0030] A thin silicon oxide layer 234 of about 5nm is thermally grown on the side of polysilicon or CVD uniformly deposited. Then a disposable polysilicon layer typically having a thickness of between about 90 to 150 nm is deposited. Then the vertical or anisotropic polysilicon etch is performed, which forms the disposable sidewall spacer 243 in Fig 6B. This is a thicker spacer than in the first and second embodiments. Then As ions are implanted at dosage of between 1E15 to 5E15 cm^2 and at the energy range of 20to 50 KeV through the composite layer of oxide-nitride in order to form an N+ junction 204. By adjusting the lateral out diffusion with annealing temperature and time (between 850 to 900°C and 5 to 20 min), the channel length defined from the edge of the word gate to the N+ junction edge is designed to be about 30 to 50 nm (3 to 4 times the electron mean free length) for ballistic high injection efficiency at low voltage.

[0031] Afterwards, the disposable side wall spacer 243 is gently removed by a dry chemical, isotropic etch. Atypical etch ambient for this step is $HBr/CL_2/O_2$. The exposed silicon oxide over nitride is gently etched out by buffered hydrofluoric acid. A fresh silicon oxide 244 replacing the top oxide in the composite ONO 230, shown in Fig. 6C, of about 4 to 6 nm is deposited by chemical vapor deposition. Thermal oxidation is added after the top layer is deposited to improve the top oxide quality.

[0032] As an option, prior to removal of the disposable sidewall spacer 243, the exposed top two layers of oxide-nitride are etched by RIE. Then the fresh oxide of about 4 to 6 nm is deposited by chemical vapor deposition and followed by thermal oxidation for the top oxide improvement. During this oxidation process of about 850 to 900 °C and 10min in wet O_2 atmosphere an extra oxide layer of about 20nm is formed on the nitride cut area over the n+ junction as shown by 244 in Fig. 6D. This thick oxide reduces the coupling capacitance between control gate 240 and bit diffusion 204.

[0033] A layer of polysilicon approximately 300 nm, which is slightly thicker than the summation of word polysilicon 245 and the top nitride 232 height, is deposited and CMP is performed using the nitride layer as the etch stop layer, Then the filled polysilicon layer 240 is recessed about 50nm by a vertical, anisotropic reactive ion etch. Then thin Ti or Co of about 10nm is deposited and silicidation is performed. The silicide layer 241 is to reduce the control gate resistance. A CVD SiO_2 deposition and CMP is performed again, as illustrated by 236. The cross section of the device at this point is shown in Fig. 6C and in Fig. 6D.

[0034] Then the nitride layer 232 is selectively etched by H_3PO_4 or etched by a chemical dry etch. The polysilicon layer 248 having a thickness of between 150 and 200 nm is deposited by CVD. This polysilicon layer and underlying word gate polysilicon 245 are defined by normal photoresist and RIE processes. The structure at this point is as Shown in Fig. 6F.

[0035] The polysilicon layer 248 acts as a word line wire by connecting adjacent word line gates. The final memory cell is completed at this point. This word polysilicon layer can be silicided with Ti or Co to reduce the sheet resistance. A typical bird's-eye view of the memory cell is shown in Fig. 4G. The shallow trench isolation region is provided by the area 209. It is understood that these critical dimensions will scale with the technology as the critical dimension is reduced.

[0036] In the embodiments described above, two approaches have been combined to improve memory density in this invention. In the first approach, density is more than doubled by sharing as many cell elements as possible. A single word select gate is shared between two nitride charge storage regions, and source lines/bit rules as well as control gate lines are shared between adjacent cells. In the second approach, multi-level thresholds are stored in the nitride regions under the control gates, and specific voltage and control conditions have been developed in order to make multi-level sensing and program possible for the high density array, with good margins between each of the threshold levels.

OPERPLTING METHOD FOR MULTILEVEL STORAGE

[0037] The procedures described below can be applied to multi-level storage of two bits or greater, as well as single-bit/two level storage applications in which Vt-hi and Vt-low are the highest and lowest threshold voltages, respectively, to be stored in the nitride region under the control gate. The dual bit nature of the memory cell comes from the association of two nitride regions paired to a single word gate and the interchangeability of source and drain regions between cells. This cell structure can be obtained by a side wall deposition process, and fabrication and operation concepts can be applied to both a step split ballistic transistor and/or a planar split gate ballistic transistor. The step split and the planar ballistic transistors have low programming voltages, fast program times, and thin oxides.

[0038] A cross-section of the array for a planar split gate ballistic transistor application is shown in Fig. 7B. All word gates 340, 341, and 342 are formed in first level polysilicon and connected together to form a word line 350. ONO is formed underneath the sidewalls 331a, 331b, 332a, 332b that are deposited in pairs on either side of the word gates 340, 341, and 342. The nitride within the ONO layer which is under each sidewall is the actual region for electron memory storage. These nitride regions are 310, 311, 312, 313, 314,315 in Figs. 7B and 7C. In order to simplify peripheral decode circuitry, two side wall control gates sharing the same diffusion will be connected together to form a single control gate 330, 331, 332, 333, according to process embodiment 3 and embodiments 1 and 2 in which the gap-filling material 247 is a conductor. In the cases of process embodiments 1 and 2 in which two side wall gates sharing a diffusion are isolated from each other (where the gap-filling material is an insulator), it is feasible to electrically connect these two gates together with a wire outside of the memory array. Although it is also possible to operate the memory array with individual sidewall gates as control gates, peripheral logic will become more cumbersome, which does not meet the interests of high density memory.

[0039] Nitride regions 311 and 312 share control gate 331, and nitride regions 313 and 314 share control gate 332. A memory cell 301 can be described as having a source diffusion 321 and bit diffusion 322, with three gates in series between the source diffusion and the bit diffusion, a control gate 331 with underlying nitride region 312, a word gate 341, and another control gate 332 with underlying nitride region 313. The word gate 341 is a simple logical ON/OFF switch, and the control gates allow individual expression of a selected nitride region's voltage state during read. Two nitride charge regions which share the same word gate will be hereinafter referred to as a "nitride charge region pair". Within a single memory cell 301, one nitride charge region 313 is selected within a nitride charge region pair for read access or program operations. The "selected nitride charge region" 313 will refer to the selected nitride region of a selected nitride pair. The "unselected nitride charge region" 312 will refer to the unselected nitride charge region of a selected nitride charge region pair. "Near adjacent nitride charge regions" 311 and 314 will refer to the nitride charge regions of the nitride charge pairs in the adjacent unselected memory cells which are closest to the selected memory cell 301, "Far unselected adjacent nitride charge regions" 310 and 315 will refer to the nitride charge regions opposite the near unselected adjacent nitride charge regions within the same unselected adjacent memory cell nitride charge region pairs. The "source" diffusion 321 of a selected memory cell will be the farther of the two memory cell diffusions from the selected nitride charge region and the junction closest to the selected nitride charge region will be referred to as the "bit" diffusion 322.

[0040] In this invention, control gate voltages are manipulated to control the behavior of an individual nitride charge region from a pair of nitride charge regions. There are three control gate voltage states; "over-ride", "express", and "suppress". A description of the control gate voltage states follows, in which the word line voltage is assumed to be 2.0V, the "bit" diffusion voltage is 0V, and the "source" diffusion voltage is assumed to be 1.2V. It should be understood that the voltages given are examples for only one of many possible applications, depending on the features of the process technology, and are not to be limiting in any way. In the over-ride state, the V(CG) is raised to a high voltage (-5V) forcing the channel under the control gate to conduct regardless of the charge stored in the nitride regions. In the express state, the control gate voltage is raised to about Vt-hi (2.0V), and the channel under the control gate will conduct, depending on the programmed state of the nitride regions. In suppress-mode, the control gate is set to 0V to suppress conduction of the underlying channels.

[0041] Table 1 gives the voltages during read of selected nitride region 313.

Table 1

Voltages for Read of Selected FG=313										
Vd0 320	Veg0 330	Vw1 340	Vd1 321	Veg1 331	Vw1 341	Vd2 322	Veg2 332	Vw1 342	Vd3 323	Veg3 333
0*	0	2.5	1.2	5	2.5	-0	2.5	2.5	0*	0

*If threshold voltage is slightly negative, it is possible to suppress the nitride threshold region with a slightly negative control gate voltage (about -0.7V)

[0042] During read operation of nitride region 313, shown in Fig. 7C, the source line 321 can be set to some intermediate voltage (-1.2V) and the bit line 322 may be precharged to 0V. In addition, the following conditions must be met in order to read a selected nitride charge region;

1) the word select gate voltage must be raised from 0V to a voltage (2.5V) which is some delta greater than the sum of the threshold voltage of the word select gate (Vt-wl=0.5V) and the source voltage (1.2V), and
2) the voltage of the control gate above the selected nitride charge region must be near Vt-hi ("express"). The voltage of the control gate above the unselected nitride charge regions must be greater than the source voltage plus Vt-hi ("over-ride"). The control gates above the unselected adjacent nitride charge regions must be zero

("suppress"). The voltage of the bit diffusion 322 can be monitored by a sense amplifier and compared to a switchable reference voltage, or several sense amplifiers each with a different reference voltage, to determine the binary value that corresponds to nitride charge region 313's threshold voltage, in a serial or parallel read manner, respectively. Thus, by over-riding the unselected nitride region within the selected memory cell, and then suppressing the adjacent cell unselected nitride regions, the threshold state of an individual selected nitride region can be determined.

[0043] For ballistic channel hot electron injection, electrons are energized by a high source-drain potential, to inject through the oxide and onto the nitride. The magnitude of the programmed threshold voltage can be controlled by the source-drab potential and the program duration. Table 2 describes the voltages to program multiple threshold voltages to a selected nitride region 313. These voltages are for example only, to facilitate description of the program method, and are not limiting in any way. In Table 2A, the control gates 331, 332 associated with the selected memory cell 301 are raised to a high voltage (5V) to over-ride the nitride charge regions 312 and 313.

Table 2A

Bit Diffusion Method Program of Selected Nitride Charge Region 313									
Vt Data	Vd0 320	Veg0 330	Vw1 340	Vd1 321	Veg1 331	Vw1 341	Vd2 322	Veg2 332	
00	0	0	2.0	-0	5	2.0	5	5	
01	0	0	2.0	-0	5	2.0	4.5	5	
10	0	0	2.0	-0	5	2.0	4.0	5	

[0044] Program of the desired threshold level is determined by the bit diffusion 322. The bit diffusion 322 is fixed to 5V, 4.5V, or 4.0V in order to program threshold voltages of 2.0v, 1.6V and 1.2V, respectively. When the word line 350 is raised above the word gate's 341 threshold, high energy electrons will be released into the channel, and injection begins. To inhibit program in the adjacent memory cells, the far adjacent control gates are set to 0V, so there will be no electrons in the channels of the adjacent memory cells. Thus, multi-level threshold program can be achieved by bit diffusion voltage control for this high density memory array. It is also possible to program multiple thresholds by varying the word line voltage, for example 4.5V, 5V and 5.5V, to program 1.2V, 1.6V and 2.0V, respectively.

[0045] Another possible method of program is to vary the control gate voltage in order to obtain different threshold levels. If multi-levels are to be obtained by control gate voltage, the unselected control gate 331 within the selected memory cell 301 will be set high to 5V in order to over-ride nitride region 312. The control gate 332 over the selected nitride region 313 will be varied to 4.5V, 5V and 5.5V, to obtain threshold voltages of 1.2V, 1.6V and 2.0V, respectively.

[0046] A fourth program method variation to the voltage conditions described for multi-level program is given in Table 2B, in which the selected control gate voltage matches the bit voltage for Vd=5V, 4.5V, and 4.0V and Vcg=5V, 4.5V, and 4.0V, respectively.

Table 2B

Control Gate-Bit Method Program of Selected Nitride Charge Region 31									
Vt Data	Vd0 320	Veg0 330	Vw1 340	Vd1 321	Veg1 331	Vw1 341	Vd2 322	Veg2 332	
00	0	0	2.0	-0	5	2.0	5	5	
01	0	0	2.0	-0	4.5	2.0	4.5	4.5	
10	0	0	2.0	-0	4.0	2.0	4.0	4.0	

[0047] Because the program current is low, and by programming schemes described above, it is possible to program several cells on the same word line in a parallel operation. Furthermore, depending on the peripheral decoding circuitry, multiple thresholds may also be programmed simultaneously, if the program methods of bit diffusion or control gate control are used. It should be noted however, that selected memory cells can have no fewer than two memory cells between each other, in order to obtain properly isolated behavior. Also, in order to obtain the tight Vt margins which are necessary for multi-level operation, the threshold voltage should be periodically checked during program, by a program verify cycle which is similar to a read operation. Program verify for the ballistic short channel sidewall MONOS in this invention is simpler than conventional floating gate and MONOS memories because program voltages are so low and very similar to read voltage conditions.

[0048] Removal of electrons from the nitride region during erase can be done by hot hole injection from the nitride region to the diffusion, or by F-N tunneling from the nitride region to the control gate. In the hot hole injection method, the substrate is grounded, diffusions are set to 5V and negative 5V is applied to the control gate. For F-N tunneling, a negative 3.5V is applied to both the substrate and diffusions and positive 5V is applied to the control gates. A block of nitride regions must be erased at once. A single nitride region cannot be erased.

PREFERRED EMBODIMENT FOR READ

[0049] Read operation for a two bit multi-level storage in each of the nitride regions will be described, based on simulations for a 0.25u process. Fig. 8A illustrates the memory cell and voltage conditions for a read of nitride charge region 313. The threshold voltages for the four levels of storage are 0.8V, 1.2V 1.6V and 2.0 for the "11", "10", and "01" and "00" states, respectively. This is shown in Fig. 8B. The threshold voltage for the word select gate is 0.5V. During read, the source voltage is fixed to 1.2V. The control gate above the unselected nitride charge region is set to 5V, which overrides all possible threshold states, and the control gate above the selected nitride charge region is set to 2.0V, which is the highest threshold voltage of all the possible threshold states. All other control gates are set to zero, and the bit junction is precharged to zero. The word line is then raised from 0V to 1.0V, and the bit junction is monitored.

[0050] Sensing the bit junction yields the curves shown in Fig. 8C. Bit line voltage sensing curves 71, 73, 75, and 77 during read of nitride charge region 313 are shown for different thresholds 0.8V, 1.2V, 1.6V, and 2.0V, respectively. It can be seen from the voltage curves, that the voltage difference between each of the states is approximately 300mV, which is well within sensing margins. Simulation has also confirmed that the sate of the unselected cell has very little impact on the bit junction voltage curve in Fig. 8C.

[0051] The present invention provides a method for forming a double side wall control gate having an ONO nitride charge storage region underneath with an ultra short channel. The enhancement mode channel is around 35nm, and is defined by the side wall spacer. The isolation between the word gates is formed by a serf-aligned SiO_2 filling technique. The polysilicon control gate is formed by a self-aligned technique using chemical mechanical polishing. The process of the invention include two embodiments; a planar short channel structure with ballistic injection and a step split short channel structure with ballistic injection. A third embodiment provides isolation of adjacent word gates after control gate definition.

[0052] While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

Industrial Applicability

[0053] According to the present invention. a fast low voltage ballistic program, ultra-short channel, ultra-high density, dual-bit multi-level flash memory is achieved with a two or three polysilicon split gate side wall process.

Claims

1. Amethod for fabricating a MONOS memory device comprising:

   forming a gate silicon oxide layer (221)on the surface of a semiconductor substrate(200);
   depositing a first polysilicon layer (245) overlying said gate silicon oxide layer;
   depositing a first nitride layer (232) overlying said first polysilicon layer;
   patterning said first polysilicon layer and said first nitride layer to from word gates wherein a gap is left between two of said word gates;
   forming a first insulating layer (234) on the sidewalls of said word gates;

depositing a spacer layer overlying said word gates and said gate silicon oxide layer;
anisotropically etching away said spacer layer (242) to leave disposable spacers on the sidewalls of said word gates;
implanting ions into said semiconductor substrate to form a lightly doped region (203) wherein said disposable spacers act as an implantation mask;
thereafter removing said disposable spacers;
depositing a nitride-containing layer (230) over said semiconductor substrate in said gap;
depositing a second polysilicon layer overlying said word gates and said nitride-containing layer;
anisotropically etching away said second polysilicon layer and said nitride-containing layer to leave polysilicon spacers on the sidewalls of said word gates wherein said polysilicon spacers form control sidewall spacer gates and wherein said nitride-containing layer underlying each of said control sidewall spacer gates forms a nitride region in which charge is stored;
forming a second insulating layer (233) on said control sidewall spacer gates (240);
implanting ions into said semiconductor substrate to form a bit diffusion region (204) wherein said control sidewall spacer gates act as an implantation mask;
coating a gap filling material (247) over the surface of said substrate wherein said gap-filling material fills said gap between said two of said word gates;
planarizing said gap-filling material;
thereafter removing said first nitride layer (232) overlying said word gates: and
depositing a third polysilicon layer (248) overlying said substrate wherein said third polysilicon layer forms a word line connecting underlying said word gates.

2. The method according to claim 1 wherein said gate silicon oxide layer (221) has a thickness of between about 5 and 10 nanometers.

3. The method according to Claim 1 wherein said first polysilicon layer (245) is depositedby chemical vapor deposition to a thickness of between about 150 and 250 nanometers.

4. The method according to claim 1 wherein said first nitride layer (232) is deposited by chemical vapor deposition to a thickness of between about 50 and 100 manometers.

5. The method according to Claim 1 wherein said first insulating layer (234) is formed by thermally growing a silicon oxide layer to a thickness of between about 5 and 10 nanometers on the sidewalls of said word gates.

6. The method according to Claim 1 wherein said first insulating layer is formed by depositing a silicon oxide layer by chemical vapor deposition to a thickness of between about 5 and 10 nanometers on the sidewalls of said word gates.

7. The method according to Claim 1 wherein said first insulating layer is formed by depositing a silicon nitride layer to a thickness of between about 5 and 10 nanometers on the sidewalls of said word gates.

8. The method according to Claim 1 wherein said first insulating layer is formed by depositing a silicon oxide layer and a silicon nitride layer to a combined thickness of between about 5 and 10 nanometers on the sidewalls of said word gates.

9. The method according to Claim 1 wherein said spacer layer (242) comprises one of the group containing polysilicon, plasma nitride, plasma oxynitride, and borophosphosilicate glass (BPSG) and has a thickness of between about 30 and 50 nanometers.

10. The method according to Claim 1 wherein said step of removing said disposable spacers comprises a dry chemical anisotropic etch.

11. The method according to Claim 1 wherein said step of depositing said nitride-containing layer (230) comprises;

growing a first silicon oxide layer to a thickness of between about 3.6 and 5.0 nanometers on said semiconductor substrate;
depositing a silicon nitride layer having a thickness of about 2 to 5 nanometers overlying said first silicon oxide layer; and

depositing a second silicon oxide layer having a thickness of between about 4 and 8 nanometers overlying said silicon nitride layer.

12. The method according to claim 1 further comprising nitriding said first silicon oxide layer before said step of depositing said silicon nitride layer.

13. The method according to Claim 1 wherein said second polysilicon layer has a thickness of between about 30 and 50 nanometers.

14. The method according to Claim 1 wherein said second polysilicon layer has a thickness of between about 30 and 50 nanometers and further comprising depositing a tungsten silicide layer having a thickness of between about 60 and 100 nanometers and wherein said second polysilicon layer and tungsten silicide layer together form said control sidewall spacer gates.

15. The method according to claim 1 wherein said second insulating layer (233) comprises silicon oxide deposited by chemical vapor deposition to a thickness of about 10 nanometers.

16. The method according to Claim 1 wherein said second insulating layer comprises silicon nitride deposited by chemical vapor deposition to a thickness of about 10 nanometers.

17. The method according to Claim 1 further comprising;

anisotropically etching said second insulating layer to form sidewall oxide spacers on lower portions of said control sidewall spacer gates (240); and
thereafter siliciding (241) upper portions of said control sidewall spacer gates and said bit diffusion region.

18. The method according to Claim 1 wherein said gap-filling material comprises one of the group containing silicon oxide and borosilicate glass.

19. The method according to Claim 1 wherein said gap-filling material comprises a conductivematerial and further comprising;

recessing said conductive material below the surface of said first nitride layer;
depositing a silicon oxide layer (236) overlying said recessed conductive material; and
planarizing said silicon oxide layer wherein said conductive material and underlying said control sidewall spacer gates together form a control gate.

20. The method according to Claim 1 wherein said third polysilicon layer (248) has a thickness of between about 150 and 200 nanometers.

21. The method according to Claim 1 further comprising siliciding said word line.

22. A method for fabricating a step split structure MONOS memory device comprising;

forming a gate silicon oxide layer (221) on the surface of a semiconductor substrate (200);
depositing a first polysilicon layer (245) overlying said gate silicon oxide layer;
depositing a first nitride layer (232) overlying said first polysilicon layer;
patterning said first polysilicon layer and said first nitride layer to form word gates wherein a gap is left between two of said word gates;
forming a first insulating layer (234) on the sidewalls of said word gates;
depositing a spacer layer overlying said word gates and said gate silicon oxide layer;
anisotropically etching away said spacer layer to leave disposable spacers (242) on the sidewalls of said word gates;
etching away said gate silicon oxide layer not covered by said word gates and said disposable spacers to expose a portion of said semiconductor substrate;
etching away said exposed portion of said semiconductor substrate to form a step into said substrate;
implanting ions into said semiconductor substrate to form a lightly doped region (203) wherein said disposable spacers act as an implantation mask;

thereafter removing said disposable spacers;
removing said gate silicon oxide layer underlying said disposable polysilicon spacers;
forming a composite layer (230) of oxide-nitride-oxide overlying said semiconductor substrate;
depositing a second polysilicon layer (240) overlying said word gates and said composite layer;
anisotropically etching away said second polysilicon layer (240) and said composite oxide-nitride-oxide layer to leave polysilicon spacers on the sidewalls of said word gates wherein said polysilicon spacers form sidewall control gates and wherein said composite oxide-nitride- oxide layer underlying each of said sidewall control gates forms a nitride region in which charge is stored;
forming a second insulating layer (233) on said control sidewall gates;
implanting ions into said semiconductor substrate to form a bit diffusion region (204) wherein said control sidewall gates act as an implantation mask;
coating a gap filling material (247) over the surface of said substrate wherein said gap-filling material fills said gap between said two of said word gates;
planarizing said gap-filling material;
thereafter removing said first nitride layer overlying said word gates; and
depositing a third polysilicon layer (248) overlying said substrate wherein said third polysilicon layer forms a word line connecting underlying said word gates.

23. The method according to Claim 22 wherein said first polysilicon layer (245) is depositedby chemical vapor deposition to a thickness of between about 150 and 250 nanometers.

24. The method according to Claim 22 wherein said first nitride layer (232) is deposited by chemical vapor deposition to a thickness of between about 50 and 100 nanometers.

25. The method according to Claim 22 wherein said first insulating layer is formed by thermally growing a silicon oxide layer to a thickness of between about 5 and 10 nanometers on the sidewalls of said word gates.

26. The method according to Claim 22 wherein said first insulating layer has a thickness of between about 5 and 10 nanometers on the sidewalls of said word gates.

27. The method according to Claim 22 wherein said spacer layer (242) comprises one of the group containing polysilicon, plasma nitride, plasma oxynitride, and borophosphosilicate glass (BPSG) and has a thickness of between about 30 and 50 nanometers.

28. The method according to Claim 22 wherein said step of removing said disposable spacers comprises a dry chemical anisotropic etch.

29. The method according to Claim 22 wherein said step into said semiconductor substrate has a depth of between about 20 and 50 nanometers.

30. The method according to Claim 22 after said step of removing said gate silicon oxide layer underlying said disposable spacers further comprising rounding the corners of said step.

31. The method according to Claim 30 wherein said step of rounding said corners of said step comprises a rapid thermal anneal at between about 1000 and 1100 °C for about 60 seconds.

32. The method according to Claim 30 wherein said step of rounding said corners of said step comprises annealing in hydrogen at about 900 °C at a pressure of between about 200 and 300 mtorr.

33. The method according to Claim 22 wherein said oxide-nitride-oxide composite layer comprises;

a first silicon oxide layer having a thickness of between about 3.6 and 5.0 nanometers;
a second silicon nitride layer having a thickness of about 2 to 5 nanometers; and
a third silicon oxide layer having a thickness of between about 4 and a nanometers,

34. The method according to Claim 22 wherein said second polysilicon layer has a thickness of between about 30 and 50 nanometers.

35. The method according to claim 22 wherein said second polysilicon layer has a thickness of between about 30 and 50 nanometers and further comprising depositing a tungsten silicide layer having a thickness of between about 60 and 100 nanometers and wherein said third polysilicon layer and tungsten silicide layer together form said control sidewall spacer gates.

36. The method according to Claim 22 wherein said second insulating layer comprises silicon oxide deposited by chemical vapor deposition to a thickness of about 10 nanometers.

37. The method according to Claim 22 wherein said second insulating layer comprises silicon nitride deposited by chemical vapor deposition to a thickness of about 10 nanometers.

38. The method according to Claim 22 further comprising;

anisotropically etching said second insulating layer to form Sidewall oxide spacers on lower portions of said control sidewall spacer gates; and
thereafter siliciding upper portions of said control sidewall spacer gates and said bit diffusion region.

39. The method according to Claim 22 wherein said gap-filling material comprises one of the group containing silicon oxide and borosilicate glass.

40. The method according to Claim 22 wherein said gap-filling material comprises a conductive material and further comprising;

recessing said conductive material below the surface of said first nitride layer;
depositing a silicon oxide layer overlying said recessed conductive material; and
planarizing said silicon oxide layer wherein said conductive material and underlying said control sidewall spacer gates together form a control gate.

41. The method according to Claim 22 wherein said third polysilicon layer has a thickness of between about 90 and 180 nanometers.

42. The method according to Claim 22 further comprising siliciding said word line.

43. The method according to Claim 22 further comprising siliciding said word line.

44. A method for fabricating a MONOS memory device comprising;

forming a nitride-containing layer (230) on the surface of a semiconductor substrate (200);
depositing a first polysilicon layer (245) overlying said nitride-containing layer;
depositing a second nitride layer (232) overlying said first polysilicon layer;
patterning said first polysilicon layer and said second nitride layer to form word gates wherein a gap is left between two of said word gates;
forming a first insulating layer (234) on the sidewalls of said word gates;
depositing a spacer layer overlying said word gates and said gate silicon oxide layer;
anisotropically etching away said spacer layer to leave disposable spacers (243) on the sidewalls of said word gates;
implanting ions into said semiconductor substrate to form a bit diffusion junction wherein said disposable spacers act as an implantation mask;
thereafter removing said disposable spacers;
depositing a second polysilicon layer (240) overlying said word gates and filling said gap;
recessing said second polysilicon layer below a surface of said second nitride layer;
siliciding (241) said recessed second polysilicon layer wherein said silicided recessed second polysilicon layer forms a control gate;
depositing an oxide layer (236) overlying said silicided (241) recessed second polysilicon layer;
thereafter removing said second nitride layer (232) overlying said word gates; and
depositing a third polysilicon layer (248) overlying said substrate wherein said third polysilicon layer forms a word line connecting underlying said word gates to complete said fabrication of said MONOS memory device.

45. The method according to Claim 44 wherein said step of forming said nitride-containing layer comprises;

growing a first silicon oxide layer to a thickness of between about 3.6 and 5.0 nanometers on said semiconductor substrate;
depositing a silicon nitride layer having a thickness of about 2 to 5 manometers overlying said first silicon oxide layer; and
depositing a second silicon oxide layer having a thickness of between about 4 and 8 nanometers overlying said silicon nitride layer.

46. The method according to Claim 45 further comprising nitriding said first silicon oxide layer before said step of depositing said silicon nitride layer.

47. The method according to Claim 44 wherein said first polysilicon layer is deposited by chemical vapor deposition to a thickness of between about 150 and 250 nanometers.

48. The method according to Claim 44 wherein said second nitride layer is deposited by chemical vapor deposition to a thickness of between about 50 and 100 nanometers.

49. The method according to claim 44 wherein said first insulating layer is formed to a thickness of between about 5 and 10 nanometers on the sidewalls of said word gates.

50. The method according to Claim 44 wherein said spacer layer comprises one of the group containing polysilicon, plasma nitride, plasma oxynitride, and borophosphosilicate glass (BPSG) and has a thickness of between about 30 and 50 nanometers.

51. The method according to Claim 44 further comprising before said step of removing said disposable spacers;

etching away said silicon oxide layer and said nitride layer on said nitride-containing layer not covered by said disposable spacers;
depositing a third silicon oxide layer overlying the area where said nitride layer is etched away to a thickness of between about 4 and 6 nanometers; and
oxidizing said third silicon oxide layer to form an oxide layer having a thickness of about 20 nanometers over area where said nitride layer is etched away whereby coupling capacitance between said control gate and said bit diffusion is reduced.

52. The method according to Claim 44 wherein said step of removing said disposable spacers comprises a dry chemical anisotropic etch.

53. The method according to Claim 44 wherein said second polysilicon layer has a thickness of between about 30 and 50 nanometers.

54. The method according to Claim 44 wherein said second insulating layer comprises silicon oxide deposited by chemical vapor deposition to a thickness of about 10 nanometers.

55. The method according to Claim 44 wherein said second insulating layer comprises silicon nitride deposited by chemical vapor deposition to a thickness of about 10 nanometers.

56. The method according to Claim 44 wherein said third polysilicon layer has a thickness of between about 150 and 200 nanometers.

57. A method for fabricating a flash memory device comprising;

providing word gates (340, 341, 342) overlying a gate silicon oxide layer on the surface of a semiconductor substrate wherein a gap is left between two of said word gates;
forming disposable spacers (242) on the sidewalls of said word gates;
implanting ions into said semiconductor substrate to form a lightly doped region (203) wherein said disposable spacers act as an implantation mask;
thereafter removing said disposable spacers;

forming sidewall polysilicon gates on the sidewalls of said word gates (240), each of said sidewall polysilicon gates having an underlying nitride-containing layer wherein the nitride region of said nitride-containing layer acts as a nitride charge region;
implanting ions into said semiconductor substrate to form a bit diffusion region (204) wherein said sidewall polysilicon gates act as an implantation mask;
forming an insulating layer (233) on said sidewall gates;
filling said gap between said two of said word gates with a second polysilicon layer (247);
recessing said second polysilicon layer;
siliciding (241) said recessed second polysilicon layer;
covering said silicided recessed second polysilicon layer with an oxide layer (236) wherein said silicided recessed second polysilicon layer along with underlying said sidewall polysilicon gates form a control gate; and
depositing a third polysilicon layer overlying said substrate wherein said third polysilicon layer (248) forms a word line connecting said word gates.

58. The method according to Claim 57 wherein said first polysilicon layer has a thickness of between about 150 and 250 nanometers.

59. The method according to Claim 57 wherein said disposable spacers comprise one of the group containing polysilicon, plasma nitride, plasma oxynitride, and borophosphosilicate glass (BPSG).

60. The method according to Claim 57 wherein said nitride-containing layer comprises a first layer of silicon oxide, a second layer of silicon nitride, and a third layer of silicon oxide.

61. The method according to Claim 57 after said step of removing said disposable spacers further comprising etching into said semiconductor substrate to form a step into said semiconductor substrate having a depth of between about 20 and 50 manometers.

62. The method according to Claim 57 further comprising rounding the corners of said step.

63. The method according to Claim 62 wherein said step of rounding said corners of said step comprises a rapid thermal anneal at between about 1000 and 1100 °C for about 60 seconds.

64. The method according to Claim 62 wherein said step of rounding said corners of said Step comprises annealing in hydrogen at about 900 °C at a pressure of between about 200 and 300 mtorr.

65. The method according to Claim 57 wherein a channel length defined from an edge of said word gate to an edge of adjacent said bit diffusion region is between about 30 and 50 nm and whereby ballistic electron injection occurs.

66. A MONOS memory cell comprising;

word gates (340, 341, 342) on the surface of a semiconductor substrate;
sidewall control gates on sidewalls of said word gate, separated from said word gates (331a, 331b, 332a, 332b) by an insulating layer;
nitride regions (311, 312, 313, 314) within an ONO layer underlying said sidewall control gates wherein electron memory storage is performed within said nitride regions;
a polysilicon word line (350) overlying and connecting said word gate with word gates in other said memory cells and overlying said sidewall control gates, separated from said sidewall control gates by an insulating layer; and
bit line diffusions within said semiconductor substrate adjacent to each of said sidewall control gates.

67. The MONOS memory cell of Claim 66 wherein each sidewall control gate is separated from a sidewall control gate of another said memory cell by an insulating layer.

68. The MONOS memory cell of Claim 66 wherein each control gate comprises a polysilicon layer between two of said word gates overlying said bit diffusion region and said sidewall control gates wherein said nitride regions underlie only said sidewall control gates.

69. The MONOS memory call of Claim 66 wherein a channel length defined from an edge of said word gate to an edge

of adjacent said bit diffusion region is between about 30 and 50 nm and whereby ballistic electron injection occurs.

70. The MONOS memory cell of Claim 66, wherein one of said nitride regions is a selected nitride region, and the other of said nitride regions is an unselected nitride region, and wherein said bit line diffusion near said selected nitride region is a bit diffusion, and said bit line diffusion near said unselected nitride region is a source diffusion, wherein a read operation of said cell is performed by;

over-riding said unselected nitride region;
providing a voltage on said word gate having a sum of the word gate threshold voltage, an overdrive voltage, and the voltage on said source diffusion;
providing a voltage on said control gate adjacent to said selected nitride region sufficient to allow for reading of the selected nitride region; and
reading said cell by measuring the voltage level on said bit diffusion.

71. The MONOS memory Cell of Claim 70 wherein said memory cell is one of many cells in a MONOS memory array, and further comprising applying a control gate voltage of 0 volts to all cells beside the cell desired to be read.

72. The MONOS memory cell of Claim 70 wherein said memory cell is one of many cells in a MONOS memory array, and further composing applying a control gate voltage of -0.7 volts to all cells beside the cell desired to be read in order to stop leakage.

73. The MONOS memory cell of Claim 66 wherein the voltage level on said bit diffusion may represent one of multiple threshold levels of said cell.

74. The MONOS memory cell of Claim 66, wherein one of said nitride regions is a selected nitride region, and the other of said nitride regions is an unselected nitride region, and wherein said bit line diffusion near said selected nitride region is a bit diffusion, and said bit line diffusion near said unselected nitride region is a source diffusion, wherein a programoperation of said cell is performed by;

providing a high voltage on said unselected control gate to over-ride said unselected nitride region;
raising the control gate voltage of said selected nitride region;
providing a fixed voltage on said bit diffusion;
providing a voltage on said word line which is greater than said word gate threshold voltage; and
lowering the voltage of said source diffusion such that current flows from said source diffusion to said bit diffusion wherein ballistic injection of electrons occurs from a channel region to said selected nitride region when current flows.

75. The MONOS memory cell of Claim 74 wherein multiple thresholds can be programmed by varying said voltage on said bit diffusion line.

76. The MONOS memory cell of Claim 74 wherein said memory cell is one of many cells in a MONOS memory array, and further comprising disabling nitride regions in adjacent cells sharing a word line by applying a control gate voltage of 0 volts to said adjacent cells.

77. The MONOS memory cell of Claim 66, wherein one of said control gates is a selected control gate and its underlying nitride region is a selected nitride region, and the other of said control gates is an unselected control gate and its underlying nitride region is an unselected nitride region, and wherein said bit line diffusion near said selected nitride region is a bit diffusion, and said bit line diffusion near said unselected nitride region is a source diffusion, wherein a program operation of said cell is performed by;

providing a high voltage on said unselected control gate to over-ride said unselected nitride region; and
varying a voltage on said selected control gate.

78. The MONOS memory cell of Claim 66 wherein said memory cell is one of many cells in a flash memory array that share a word line, and further comprising simultaneously programming several of said cells with different threshold levels by varying the voltage either of said control gate or said bit diffusion.

79. The MONOS memory cell of Claim 66, wherein an erase operation of a block of nitride regions is performed by;

providing a positive voltage to said bit line diffusions; and
providing a negative voltage to said control gates over said bit tine diffusions.

80. The MONOS memory cell of Claim 66, wherein an erase operation of a block of nitride regions is performed by;

providing a negative voltage to said semiconductor substrate and to said bit line diffusions; and providing a positive voltage to said control gates.

81. A method of reading a MONOS memory cell, wherein the MONOS memory cell comprises;

word gates (340, 341, 342) on the surface of a semiconductor substrate;
sidewall control gates (331a, 331b, 332a, 332b) on sidewalls of said word gate, separated from said word gates by an insulating layer;
nitride regions (311, 312, 313, 314) within an ONO layer underlying said sidewall control gates wherein electron memory storage is performed within said nitride regions;
a polysilicon word line (350) overlying and connecting said word gate with word gates in other said memory cells and overlying said sidewall control gates, separated from said sidewall control gates by an insulating layer; and
bit line diffusions (322) within said semiconductor substrate adjacent to each of said sidewall control gates,

wherein one of said nitride regions is a selected nitride region, and the other of said nitride regions is an unselected nitride region, and wherein said bit line diffusion near said selected nitride region is a bit diffusion, and said bit line diffusion near said unselected nitride region is a source diffusion,
wherein a read operation of said cell is performed by;

over-riding said unselected nitride region;
providing a voltage on said word gate having a sum of the word gate threshold voltage, an overdrive voltage, and the voltage on said source diffusion;
providing a voltage on said control gate adjacent to said selected nitride region sufficient to allow for reading of the selected nitride region; and
reading said cell by measuring the voltage level on said bit diffusion.

82. A method of programming a MONOS memory cell, wherein said MONOS memory cell comprises;

word gates (340, 341, 342) on the surface of a semiconductor substrate;
sidewall control gates (331a, 331b, 332a, 332b) onsidewalls of said word gate, separated from said word gates by an insulating layer;
nitride regions (311, 312, 313, 314) within an ONO layer underlying said sidewall control gates wherein electron memory storage is performed within said nitride regions;
a polysilicon word line (350) overlying and connecting said word gate with word gates in other said memory cells and overlying said sidewall control gates, separated from said sidewall control gates by an insulating layer; and
bit line diffusions (322) within said semiconductor substrate adjacent to each of said sidewall control gates;

wherein one of said control gates is a selected control gate and its underlying nitride region is a selected nitride region, and the other of said control gates is an unselected control gate and its underlying nitride region is an unselected nitride region, and wherein said bit line diffusion near said selected nitride region is a bit diffusion, and said bit line diffusion near said unselected nitride region is a source diffusion,
wherein said method of programming the cell comprises the steps of;

providing a high voltage on said unselected control gate to over-ride said unselected nitride region; and
varying a voltage on said selected control gate.

83. A method of erasing a MONOS memory cell, wherein said MONOS memory cell comprises;

a word gate (340) on the surface of a semiconductor substrate;
sidewall control gates on sidewalls of said word gate, separated from said word gates by an insulating layer;
nitride regions (311, 312, 313, 314) within an ONO layer underlying said sidewall control gates wherein electron

memory storage is performed within said nitride regions;
a polysilicon word line (350) overlying and connecting said word gate with word gates in other said memory cells and overlying said sidewall control gates, separated from said sidewall control gates by an insulating layer; and
bit line diffusions (322) within said semiconductor substrate adjacent to each of said sidewall control gates;

wherein said method of erasing a block of said nitride regions comprises the steps of;

providing a positive voltage to said bit line diffusions; and
providing a negative voltage to said control gate over said bit line diffusions.

84. A flash memory device comprising;

word gates (340, 341, 342) on the surface of a semiconductor substrate;
sidewall control gates (331a, 331b, 332a, 332b) on the sidewalls of said word gates separated from said word gates by an insulating layer;
bit line diffusions (322) .within said semiconductor substrate between two of said sidewall control gates; and
nitride charge regions (311, 312, 313, 314) underlying said sidewall control gates.

85. The device according to Claim 84 further comprising;

an insulating layer overlying said sidewall control gates; and
a word line overlying said control gates and connecting said word gates.

86. The MONOS memory call of Claim 84 wherein a channel length defined from an edge of said word gate to an edge of adjacent said bit diffusion region is between about 30 and 50 nm and whereby ballistic electron injection occurs.

Amended claims under Art. 19.1 PCT

66. (Canceled)

67. (Amended) A MONOS memory cell comprising;

word gates (340, 341, 342) on the surface of a semiconductor substrate;
sidewall control gates on sidewalls of said word gate, separated from said word gates (331a, 331b, 332a, 332b) by an insulating layer;
nitride regions (311, 312, 313, 314) within an ONO layer underlying said sidewall control gates wherein electron memory storage is performed within said nitride regions;
a polysilicon word line (350) overlying and connecting said word gate with word gates in other said memory cells and overlying said sidewall control gates, separated from said sidewall control gates by an insulating layer; and
bit line diffusions within said semiconductor substrate adjacent to each of said sidewall control gates; wherein each sidewall control gate is separated from a sidewall control gate of another said memory cell by an insulating layer.

69. (Amended) The MONOS memory call of Claims 67 and 68, wherein a channel length defined from an edge of said word gate to an edge of adjacent said bit diffusion region is between about 30 and 50 nm and whereby ballistic electron injection occurs.

70. (Canceled)

71. (Canceled)

72. (Amended) The MONOS memory cell of Claims 67 and 68, wherein one of said nitride regions is a selected nitride region, and the other of said nitride regions is an unselected nitride region, and wherein said bit line diffusion near said selected nitride region is a bit diffusion, and said bit line diffusion near said unselected nitride region is a source diffusion, wherein a read operation of said cell is performed by;

over-riding said unselected nitride region;
providing a voltage on said word gate having a sum of the word gate threshold voltage and the voltage on said source diffusion;
providing a voltage on said control gate adjacent to said selected nitride region sufficient to allow for reading of the selected nitride region; and
reading said cell by measuring the voltage level on said bit diffusion; wherein
said memory cell is one of many cells in a MONOS memory array, and further composing applying a control gate voltage of -0.7 volts to all cells beside the cell desired to be read in order to stop leakage.

73. (Amended) The MONOS memory cell of Claims 67 and 68, wherein one of said nitride regions is a selected nitride region, and the other of said nitride regions is an unselected nitride region, and wherein said bit line diffusion near said selected nitride region is a bit diffusion, and said bit line diffusion near said unselected nitride region is a source diffusion, wherein a read operation of said cell is performed by;

over-riding said unselected nitride region;
providing a voltage on said word gate having a sum of the word gate threshold voltage and the voltage on said source diffusion;
providing a voltage on said control gate adjacent to said selected nitride region sufficient to allow for reading of the selected nitride region; and
reading said cell by measuring the voltage level on said bit diffusion; wherein
the voltage level on said bit diffusion may represent one of multiple threshold levels of said cell.

74. (Canceled)

75. (Amended) The MONOS memory cell of Claims 67 and 68, wherein one of said nitride regions is a selected nitride region, and the other of said nitride regions is an unselected nitride region, and wherein said bit line diffusion near said selected nitride region is a bit diffusion, and said bit line diffusion near said unselected nitride region is a source diffusion, wherein a program operation of said cell is performed by;

providing a high voltage on said unselected control gate to over-ride said unselected nitride region;
raising the control gate voltage of said selected nitride region;
providing a fixed voltage on said bit diffusion;
providing a voltage on said word line which is greater than said word gate threshold voltage; and
lowering the voltage of said source diffusion such that current flows from said source diffusion to said bit diffusion wherein ballistic injection of electrons occurs from a channel region to said selected nitride region when current flows; wherein
multiple thresholds can be programmed by varying said voltage on said bit diffusion line.

76. (Canceled)

77. (Amended) The MONOS memory cell of Claims 67 and 68, wherein one of said control gates is a selected control gate and its underlying nitride region is a selected nitride region, and the other of said control gates is an unselected control gate and its underlying nitride region is an unselected nitride region, and wherein said bit line diffusion near said selected nitride region is a bit diffusion, and said bit line diffusion near said unselected nitride region is a source diffusion, wherein a program operation of said cell is performed by;

providing a high voltage on said unselected control gate to over-ride said unselected nitride region; and
varying a voltage on said selected control gate to program multiple thresholds.

78. (Amended) The MONOS memory cell of Claims 67 and 68 wherein said memory cell is one of many cells in a flash memory array that share a word line, and further comprising simultaneously programming several of said cells with different threshold levels by varying the voltage either of said control gate or said bit diffusion.

79. (Canceled)

80. (Canceled)

81. (Amended) A method of reading a MONOS memory cell, wherein the MONOS memory cell comprises;

word gates (340, 341, 342) on the surface of a semiconductor substrate;
sidewall control gates (331a, 331b, 332a, 332b) on sidewalls of said word gate, separated from said word gates by an insulating layer;
nitride regions (311, 312, 313, 314) within an ONO layer underlying said sidewall control gates wherein electron memory storage is performed within said nitride regions;
a polysilicon word line (350) overlying and connecting said word gate with word gates in other said memory cells and overlying said sidewall control gates, separated from said sidewall control gates by an insulating layer; and
bit line diffusions (322) within said semiconductor substrate adjacent to each of said sidewall control gates,

wherein one of said nitride regions is a selected nitride region, and the other of said nitride regions is an unselected nitride region, and wherein said bit line diffusion near said selected nitride region is a bit diffusion, and said bit line diffusion near said unselected nitride region is a source diffusion,
wherein a read operation of said cell is performed by;

over-riding said unselected nitride region;
providing a voltage on said word gate having a sum of the word gate threshold voltage and the voltage on said source diffusion;
providing a voltage on said control gate adjacent to said selected nitride region sufficient to allow for reading of the selected nitride region; and
measuring the voltage level on said bit diffusion.

82. (Amended) A method of programming a MONOS memory cell, wherein said MONOS memory cell comprises;

word gates (340, 341, 342) on the surface of a semiconductor substrate;
sidewall control gates (331a, 331b, 332a, 332b) on sidewalls of said word gate, separated from said word gates by an insulating layer;
nitride regions (311, 312, 313, 314) within an ONO layer underlying said sidewall control gates wherein electron memory storage is performed within said nitride regions;
a polysilicon word line (350) overlying and connecting said word gate with word gates in other said memory cells and overlying said sidewall control gates, separated fromsaid sidewall control gates by an insulating layer; and
bit line diffusions (322) within said semiconductor substrate adjacent to each of said sidewall control gates;

wherein one of said nitride region is a selected nitride region, and the other of said nitride region is an unselected nitride region, and wherein said bit line diffusion near said selected nitride region is a bit diffusion, and said bit line diffusion near said unselected nitride region is a source diffusion,
wherein said method of programming the cell comprises the steps of;

providing a high voltage on said unselected control gate to over-ride said unselected nitride region; and
varying a voltage on said selected control gate.

83. (Canceled)

84. (Canceled)

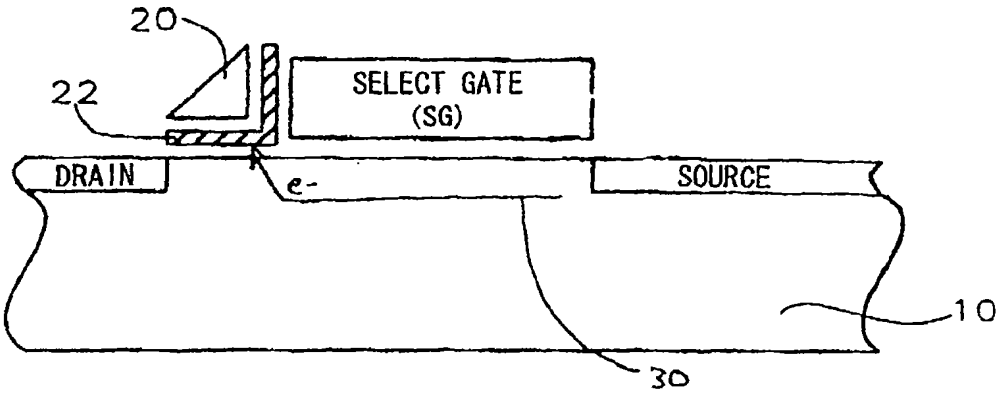
85. (Canceled)

86. (Canceled)

87. (Added) A method of programming a MONOS memory cell of claim 82, wherein program operation of said cell is performed by varying a voltage on said selected control gate.

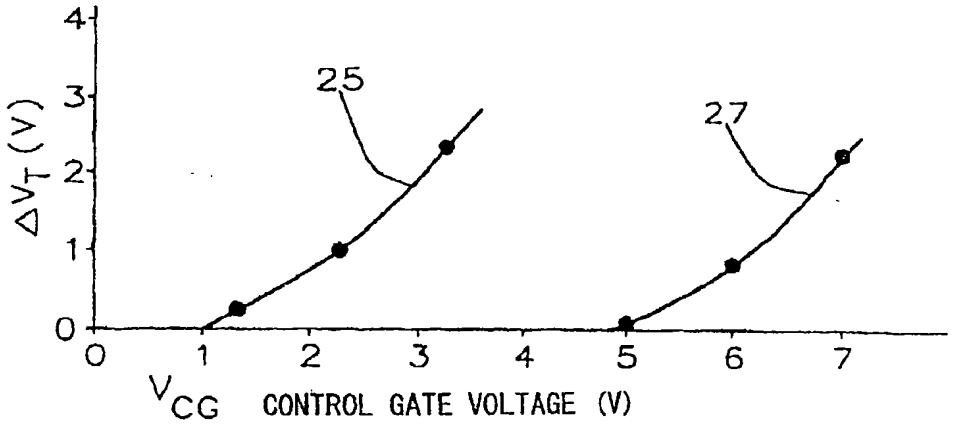
88. (Added) A method of programming a MONOS memory cell of claim 82 further comprising similar steps to said read operation performed in said program operation of said selected nitride region to detect threshold level.

Fig. 1



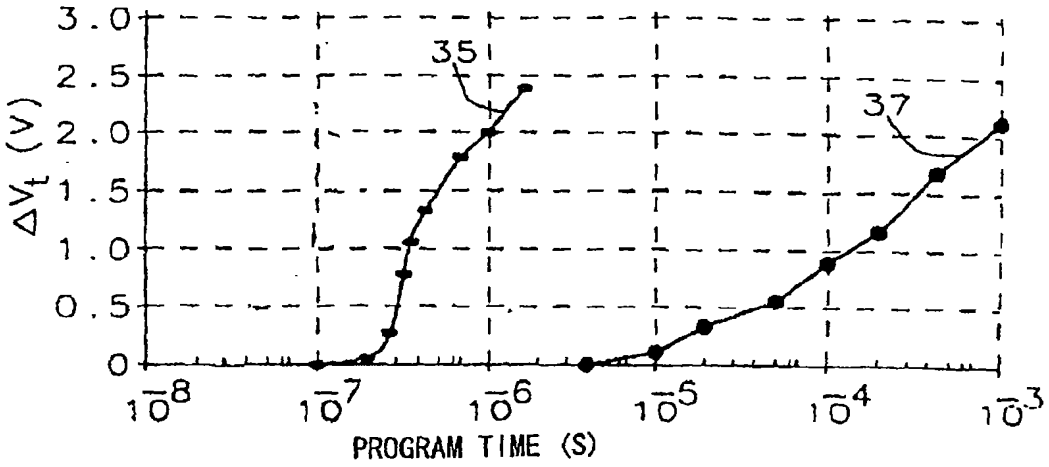
PRIOR ART

Fig. 2A



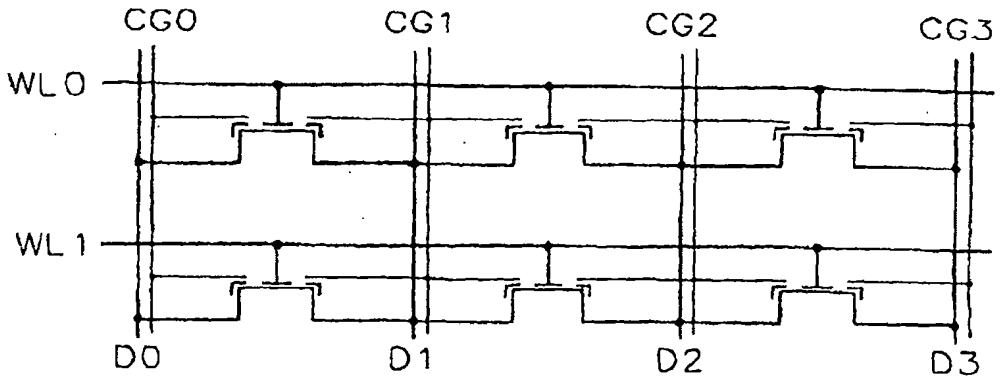
PRIOR ART

Fig. 2B



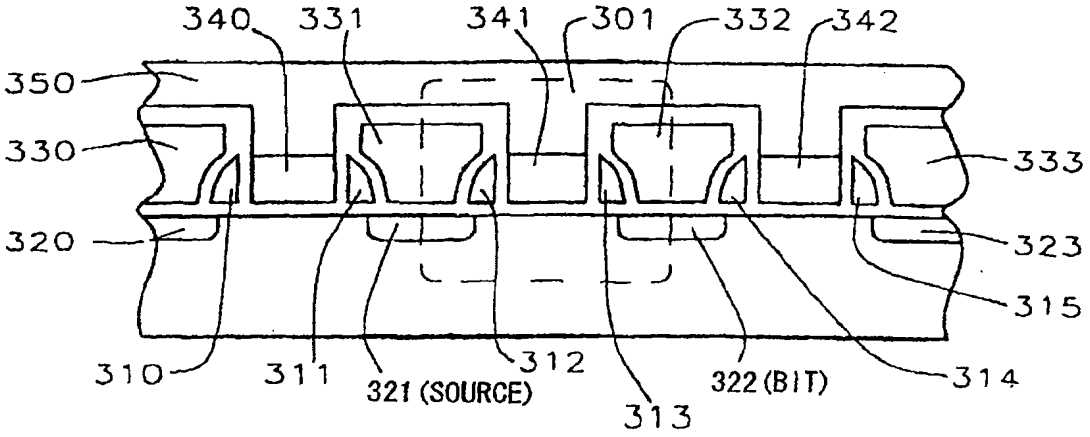
PRIOR ART

Fig. 3A



PRIOR ART

Fig. 3B



PRIOR ART

Fig. 4A

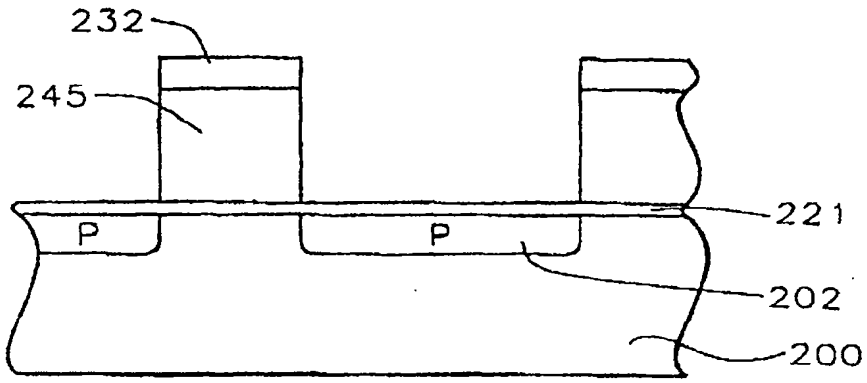


Fig. 4B

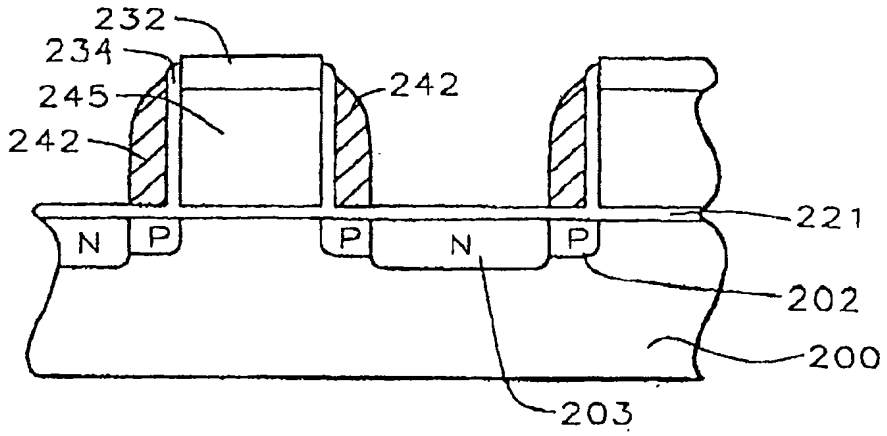


Fig. 4C

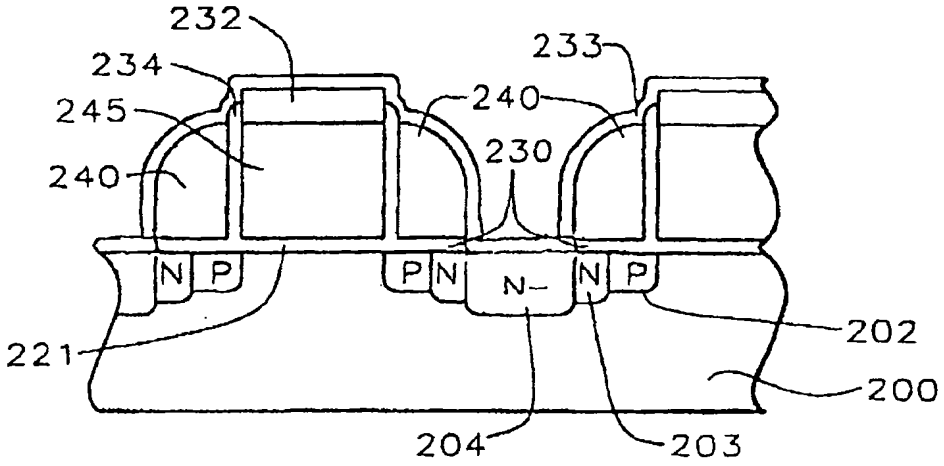

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Fig. 4D

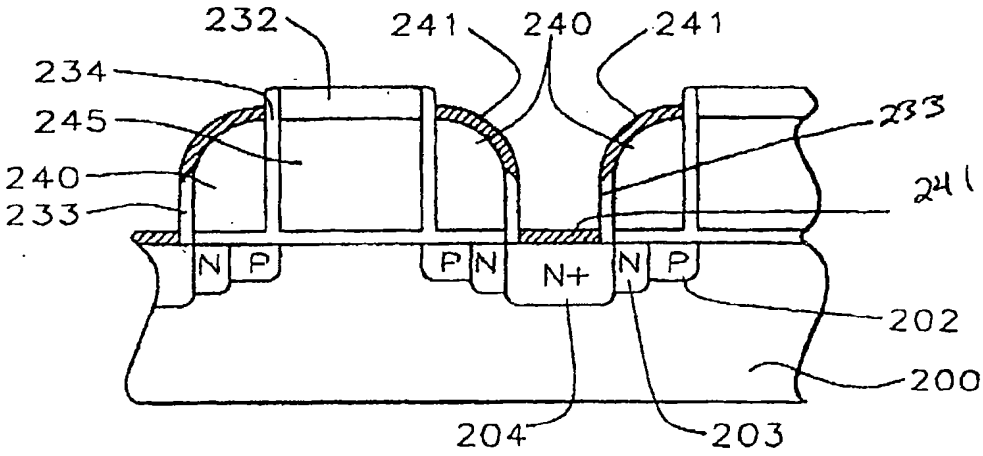
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Fig. 4E

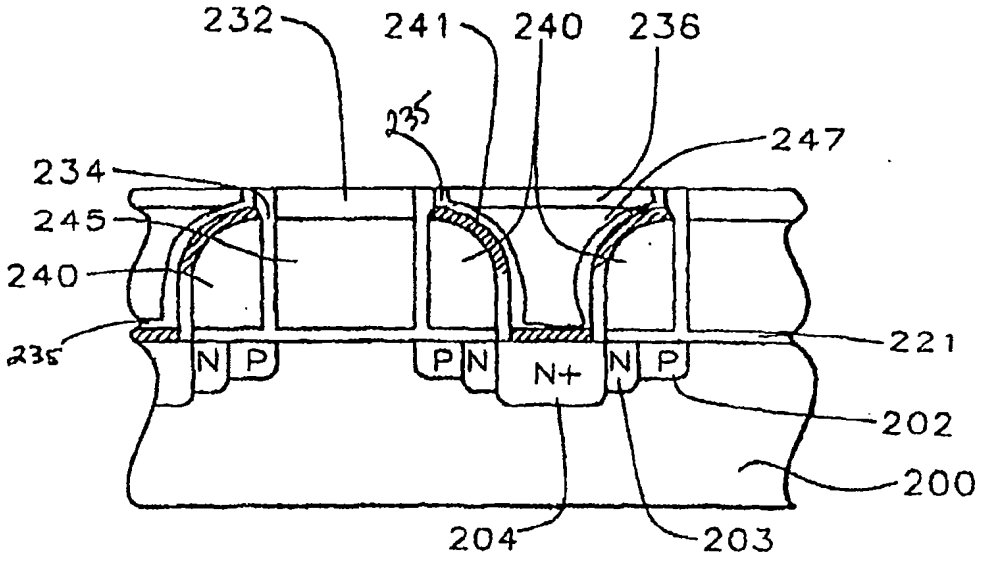
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Fig. 4F

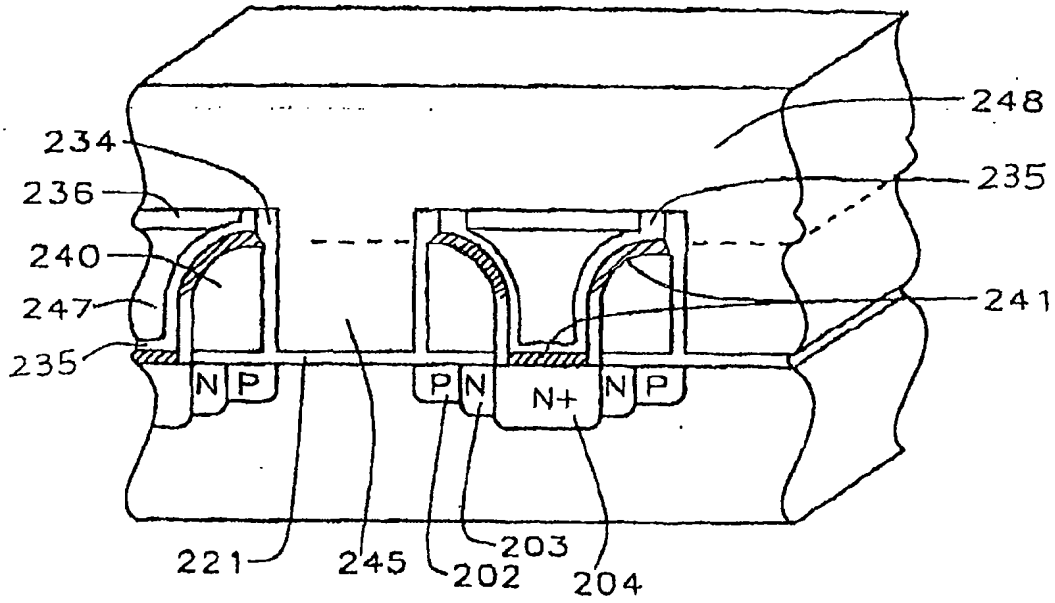
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Fig. 4G

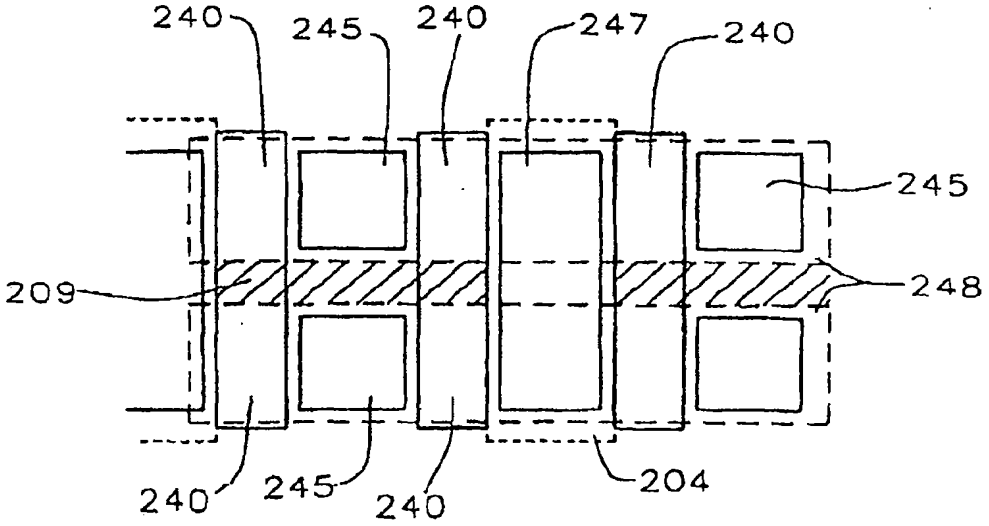

Fig. 5B

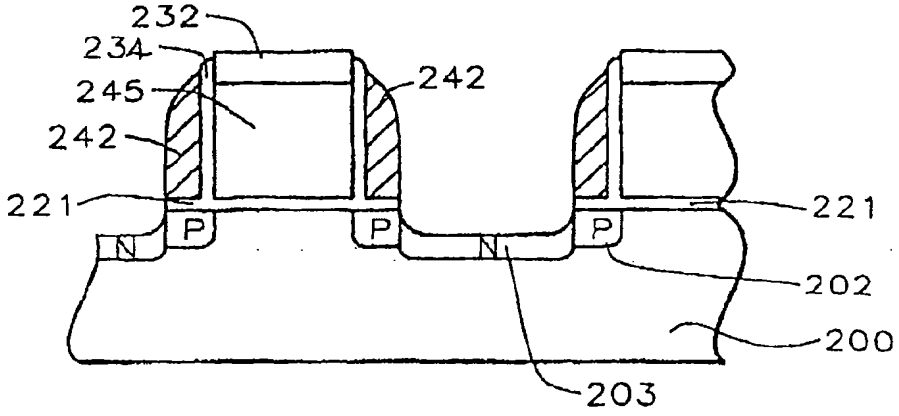

Fig. 5C

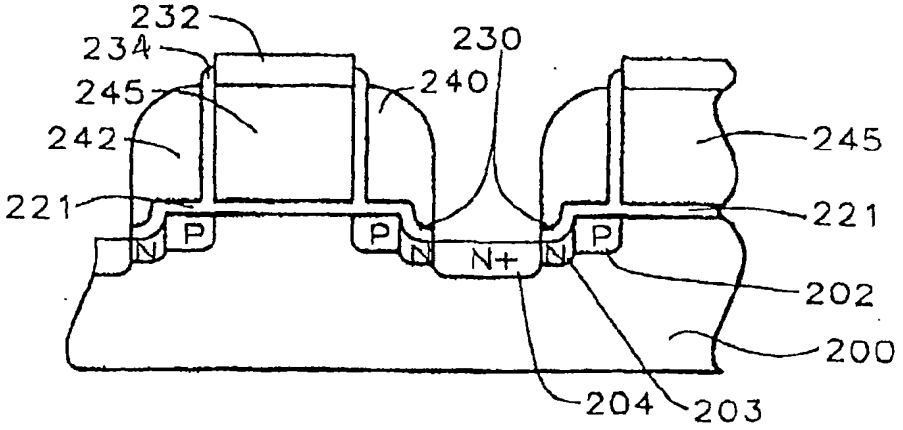

Fig. 5F

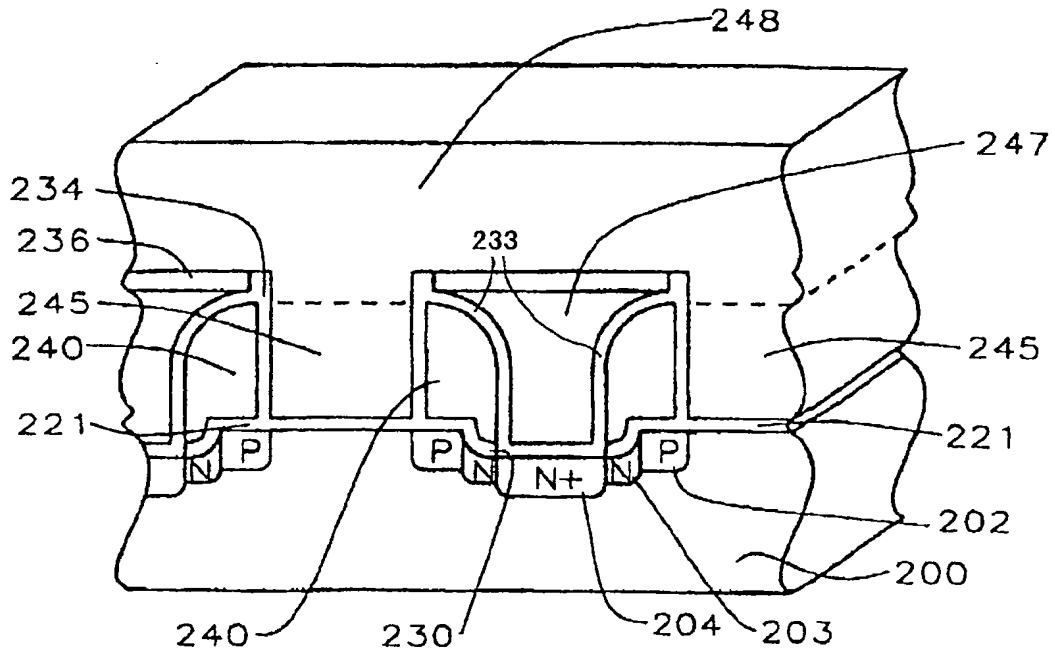
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Fig. 6A

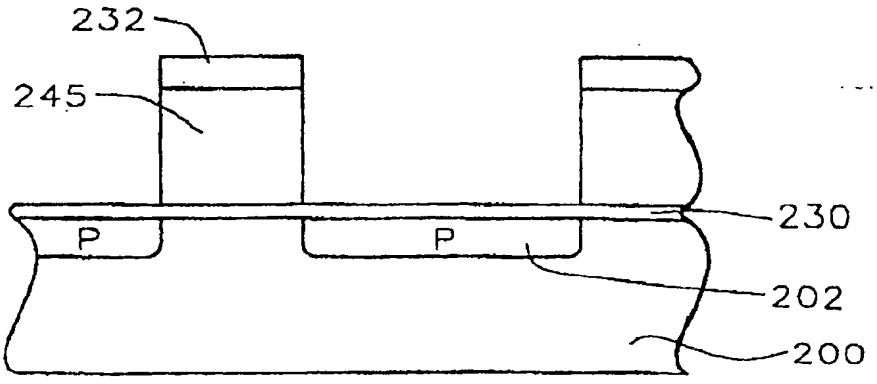
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Fig. 6B

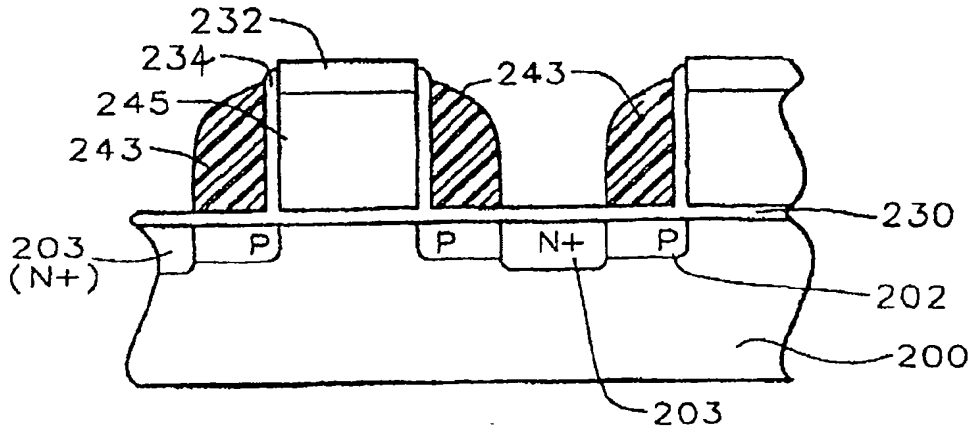

Fig. 6C

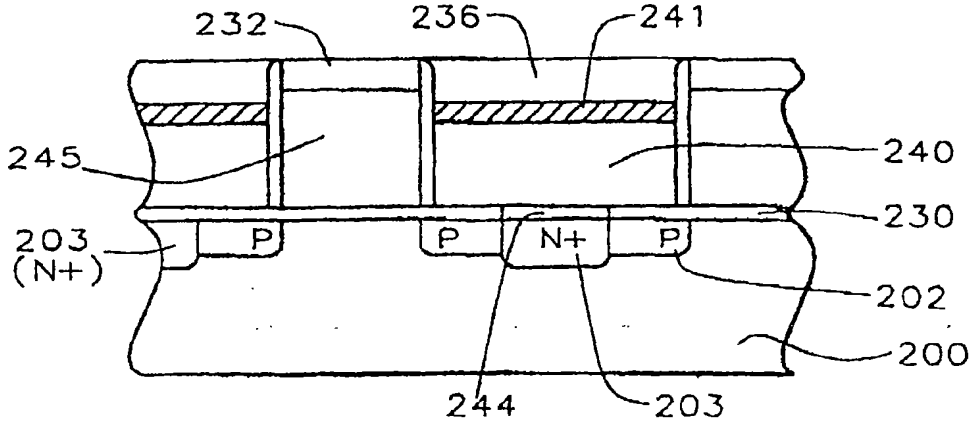

Fig. 6D

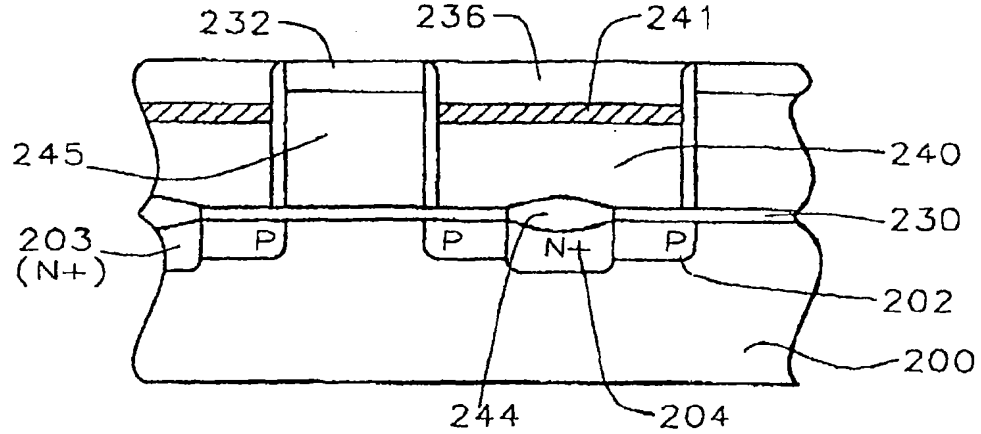

Fig. 6F

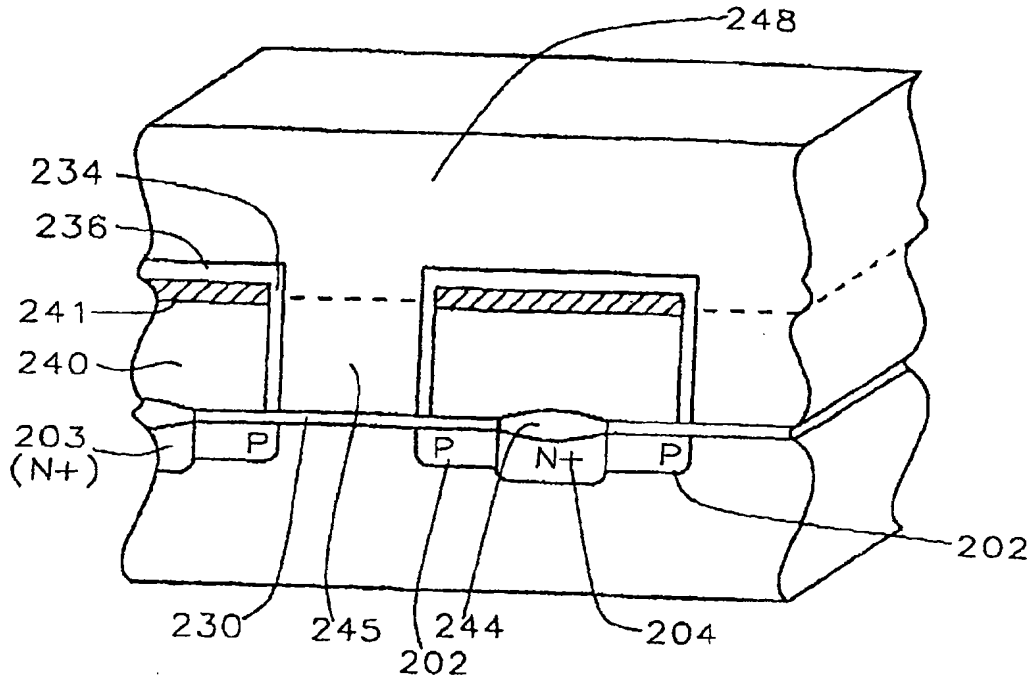
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Fig. 7A

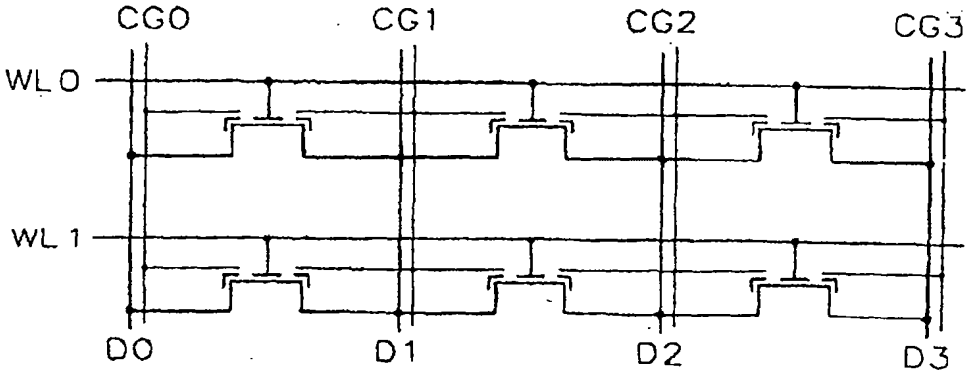
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Fig. 7B

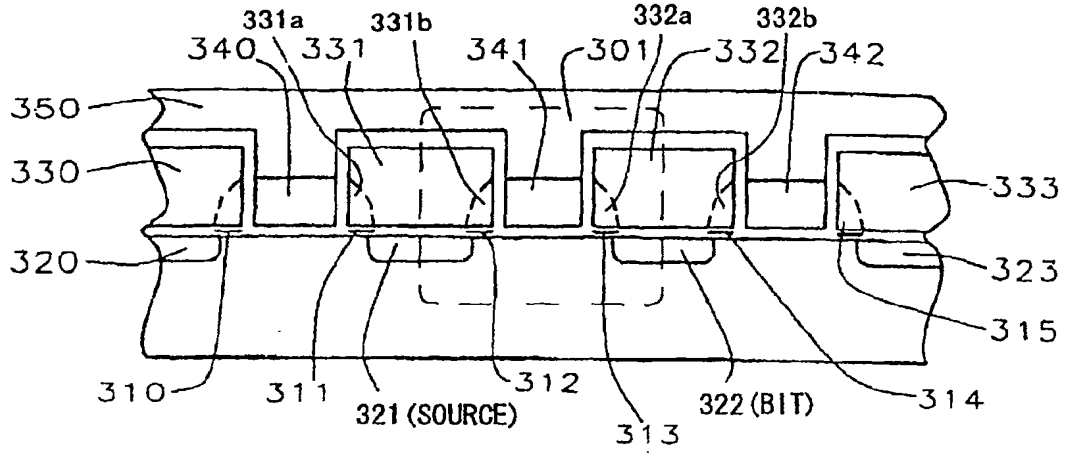

Fig. 7C

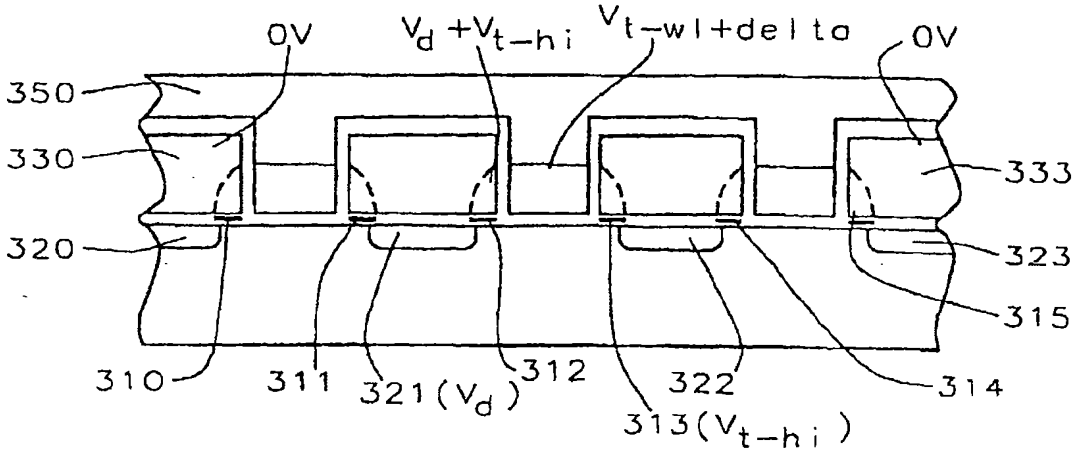

Fig. 8A

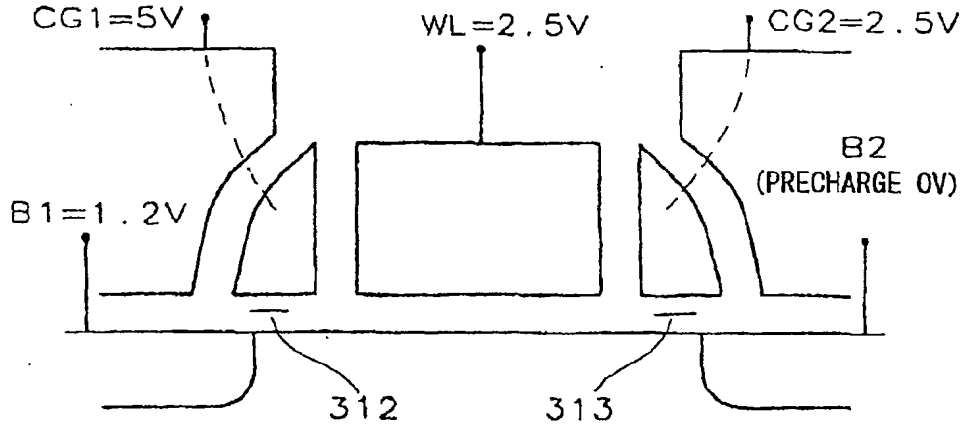

Fig. 8B

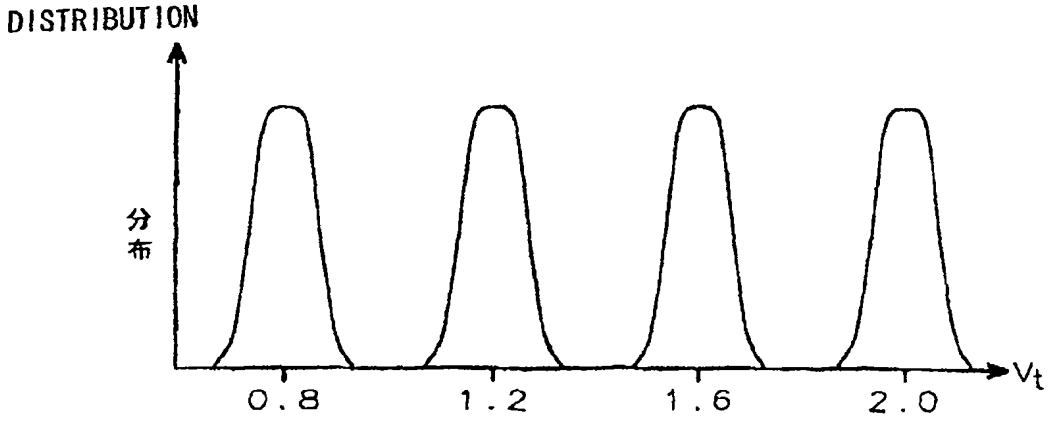
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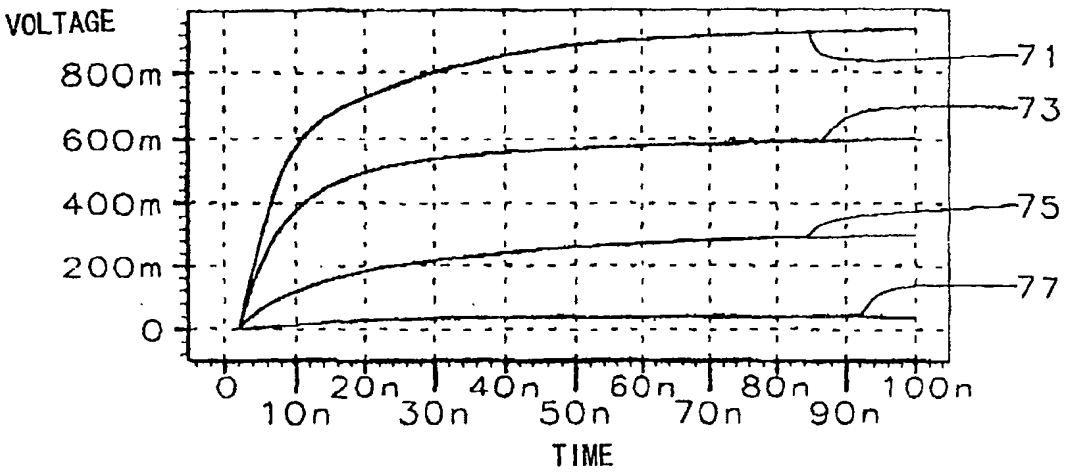
Fig. 8C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INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP01/10156

A. CLASSIFICATION OF SUBJECT MATTER
Int.Cl[7] H01L29/792, 21/8247

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int.Cl[7] H01L29/792, 29/788, 27/115, 21/8247

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Jitsuyo Shinan Koho 1926-1996 Jitsuyo Shinan Toroku Koho 1996-2002
Kokai Jitsuyo Shinan Koho 1971-2002 Toroku Jitsuyo Shinan Koho 1994-2002

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
The IEEE/IEE Electronic Library Online

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	2000 Symposium on VLSI Technology Digest of Technical Papers, 13 June, 2000 (13.06.2000), pages 122 to 123 Full text	66-68,70,73, 77-79,81-85
Y	Full text	69,71,72, 74-76,80,86
A	Full text	1-65
Y	International Electron Devices Meeting, (1998), pages 987 to 990; page 987, "Step Split Device with Ballistic Direct Injection"	69,86
Y	JP 5-145080 A (Kawasaki Steel Corporation), 11 June, 1993 (11.06.1993), Par. No. [0009] to [0012]; Figs. 1 to 4 (Family: none)	66-69,84-85

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier document but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
18 February, 2002 (18.02.02)	26 February, 2002 (26.02.02)
Name and mailing address of the ISA/ Japanese Patent Office	Authorized officer
Facsimile No.	Telephone No.

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP01/10156

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 5-326976 A (Rohm Co., Ltd.), 10 December, 1993 (10.12.1993), Par. No. [0025] to [0028]; Figs. 1 to 10 (Family: none)	1-65
EY	JP 2001-357681 A (Sony Corporation), 26 December, 2001 (26.12.2001), Full text; Figs. 2, 3, 5, 6, 9 to 11 (Family: none)	66-69,84-85
EA	JP 2001-168219 A (Sony Corporation), 22 June, 2001 (22.06.2001), Full text (Family: none)	69,86

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